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BTEC & CGLI GUIDANCE FOR STUDENTS

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CITY AND GUILDS OF LONDON INSTITUTE Telecommunications Technicians (New) Scheme

The following questions are from examination papers set for the City and Guilds of London Institute's (CGLI's) new 271 Telecommunications Technicians Scheme, and are reproduced with the permission of the CGLI. The answers given have been prepared by independent authors. Answers to some questions are occasionally omitted because of insufficient space. Students studying BTEC courses may find that these questions are useful for revision.

CGLI: ELECTRONICS T3 (1985)

Students were required to answer six questions. The time allowed was three hours. Students are advised to read the notes above

Q1 The following Tables 1 and 2 show experimental data for a particular common-emitter connected transistor, each plotted with the collector-emitter voltage V_{CE} constant at 5 V.

Table 1

Base-emitter voltage V_{BE} (volts)	0.1	0.2	0.3	0.35	0.4	0.45
Base current I_B (μA)	0	2.5	12.5	25.0	45.0	75.0

Table 2

Base current I_B (μA)	10	20	30	45	60
Collector current I_C (mA)	0.8	1.4	1.95	2.8	3.6

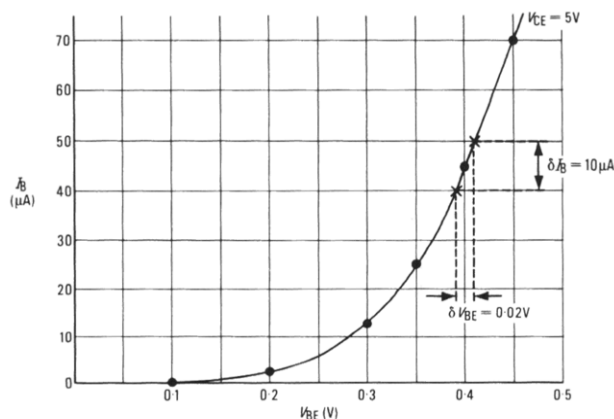
- (a) Using the data given in the tables, plot
- the input characteristic (I_B against V_{BE}), and
 - the transfer characteristic (I_C against I_B) for V_{CE} constant at 5 V.
- (b) For DC conditions $V_{CE} = 5$ V and $I_B = 45 \mu A$, determine the values of the following hybrid parameters
- h_{ie}
 - h_{fe}
 - h_{ie}
 - h_{fe}
- (c) Draw the common-emitter small-signal equivalent circuit for the transistor having parameter values obtained in (b) and determine its voltage gain for a collector load resistance of 2 k Ω (h_{oe} and h_{re} may be neglected).

A1 (a) (i) See sketch (a).
(ii) See sketch (b).

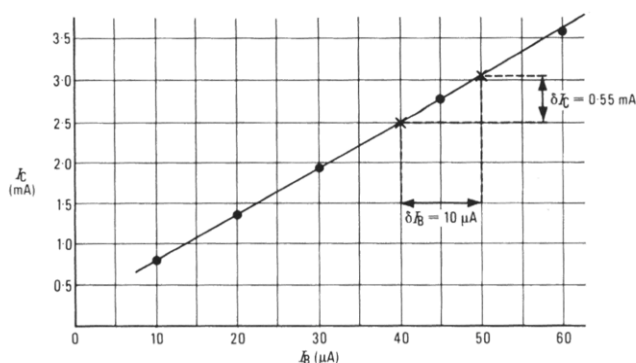
$$(b) (i) h_{ie} = \frac{\delta V_{BE}}{\delta I_B} (V_{CE} \text{ constant}) = \frac{0.02}{10 \times 10^{-6}} = 2 \text{ k}\Omega.$$

$$(ii) h_{fe} = \frac{\delta I_C}{\delta I_B} (V_{CE} \text{ constant}) = \frac{0.55 \times 10^{-3}}{10 \times 10^{-6}} = 55.$$

$$(iii) h_{ie} = \frac{V_{BE}}{I_B} (V_{CE} \text{ constant}) = \frac{0.4}{45 \times 10^{-6}} = 8.9 \text{ k}\Omega.$$



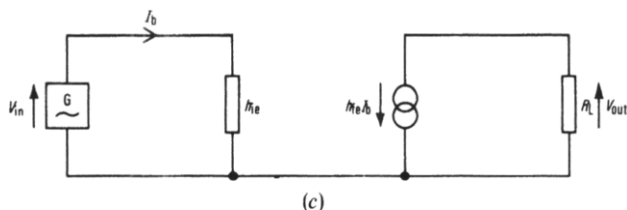
(a)



(b)

$$(iv) \quad h_{FE} = \frac{I_C}{I_B} (V_{CE} \text{ constant}) = \frac{2.8 \times 10^{-3}}{45 \times 10^{-6}} = 62.$$

(c) The common-emitter small-signal equivalent circuit is shown in sketch (c).



$$I_b = \frac{V_{in}}{h_{ie}}$$

$$V_{out} = -h_{fe} I_b R_L$$

$$\therefore V_{out} = -h_{fe} \frac{V_{in}}{h_{ie}} R_L$$

$$\therefore \text{voltage gain, } \frac{V_{out}}{V_{in}} = \frac{-h_{fe} R_L}{h_{ie}}$$

Substituting $h_{fe} = 55$, $h_{ie} = 2 \text{ k}\Omega$ and $R_L = 2 \text{ k}\Omega$ gives

$$\text{voltage gain} = \frac{-55 \times 2 \times 10^3}{2 \times 10^3} = -55.$$

Q2 The circuit of a two-stage common-source amplifier is shown in Fig. 1. Each of the two FETs has a mutual conductance (g_m) of 3.2 mS and a drain slope resistance (r_{ds}) of $40 \text{ k}\Omega$.

(a) Assuming all the capacitors shown have negligible reactance at the operating frequency, determine the RMS values of V_{OUT} if $V_{IN} = 1.5 \text{ mV}$ RMS.

(b) With reference to the circuit diagram:

- from the symbols identify the type of FET used;
- state briefly the purpose of the two $2.2 \text{ k}\Omega$ source resistors and C_3 ; and
- explain how the removal of the source capacitor C_2 would affect the overall voltage gain of the amplifier.

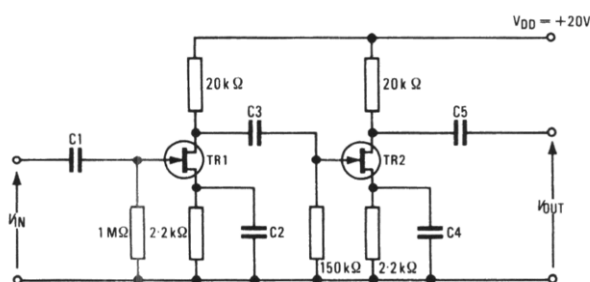
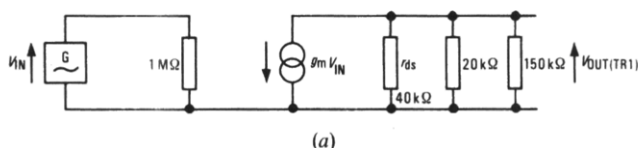


Fig. 1

A2 (a) The equivalent circuit of the first stage, between the input V_{IN} and the gate of transistor TR2, is as shown in sketch (a).



$$V_{OUT(TR1)} = -g_m V_{IN} R_T$$

where R_T is the equivalent value of the three resistance values in parallel.

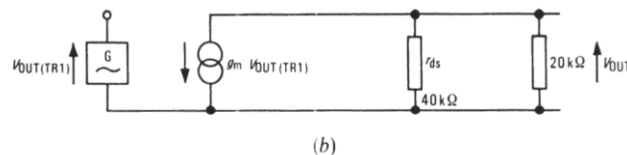
$$\frac{1}{R_T} = \frac{1}{40} + \frac{1}{20} + \frac{1}{150} \quad (\text{where } R_T \text{ is in kilohms}).$$

$$\therefore \frac{1}{R_T} = \frac{3.75 + 7.5 + 1}{150} = \frac{12.25}{150}$$

$$\therefore R_T = \frac{150}{12.25} \text{ k}\Omega.$$

$$\begin{aligned} \therefore V_{OUT(TR1)} &= -3.2 \times 10^{-3} \times V_{IN} \times \frac{150}{12.25} \times 10^3, \\ &= -39.18 V_{IN} \text{ volts,} \\ &= -39.18 \times 1.5 \text{ mV} = -58.77 \text{ mV.} \end{aligned}$$

The equivalent circuit of the second stage, between the gate of transistor TR2 and V_{OUT} , is shown in sketch (b).



$$V_{OUT} = -g_m V_{OUT(TR1)} R_T$$

where R_T is the equivalent value of the two resistance values in parallel.

$$\frac{1}{R_T} = \frac{1}{40} + \frac{1}{20} \quad (\text{where } R_T \text{ is in kilohms}).$$

$$\therefore \frac{1}{R_T} = \frac{1+2}{40} = \frac{3}{40}$$

$$\therefore R_T = \frac{40}{3} \text{ k}\Omega.$$

$$\begin{aligned} \therefore V_{OUT} &= -3.2 \times 10^{-3} \times V_{OUT(TR1)} \times \frac{40}{3} \times 10^3 \text{ volts,} \\ &= -42.66 V_{OUT(TR1)}, \\ &= -42.66 \times (-58.77) \text{ mV,} \\ &= 2507 \text{ mV.} \end{aligned}$$

(b) (i) p-gate n-channel junction-gate field-effect transistor (JUGFET).
(ii) The $2.2 \text{ k}\Omega$ source resistors provide the gate-to-source negative bias voltage owing to the potential difference developed by the quiescent drain currents which flow through them. Capacitor C_3 is the coupling capacitor between the two stages; it isolates the DC component of the drain voltage of transistor TR1 from the gate of transistor TR2, but, because it has a low reactance to the signal components, it enables the signal voltage to be developed at the gate of TR2.

(iii) If capacitor C_2 is removed, then the signal component of the drain current of transistor TR1 would develop a potential difference across the $2.2 \text{ k}\Omega$ source resistor. This potential difference would be in antiphase to the input signal voltage, and so the output of transistor TR1 is reduced. Thus the overall voltage gain of the amplifier is reduced.

[Tutorial Note: The removal of capacitor C_2 is a method of introducing negative feedback into the TR1 stage with a consequential loss of gain.]

Q3 (a) Explain with the aid of sketches the meaning of

- Class A,
- Class B, and
- Class C

amplifier bias conditions.

(b) State an application of EACH of the bias conditions listed in (a).

(c) For EACH application given in (b), explain why the particular form of bias is used.

A3 (a) (i) See sketch (a).

Class A bias is such that the quiescent operating point ($I_{C(Q)}$, $V_{BE(Q)}$) permits a 360° angle of flow of output current; that is, the output current flows at all times. The peak value of the signal must therefore always be less than the quiescent (bias) values of current and voltage.

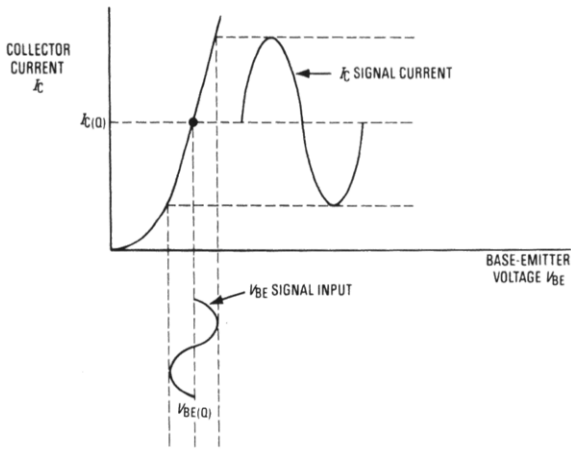
(ii) See sketch (b).

Class B bias permits a 180° angle of flow of output current; that is, the output current flows for one half cycle of the input only, and is cut off for the other half cycle. The quiescent (bias) point is therefore at the end of the characteristic; that is, the cut-off point. A disadvantage of this method is distortion due to the lower bend in the characteristic.

(iii) See sketch (c).

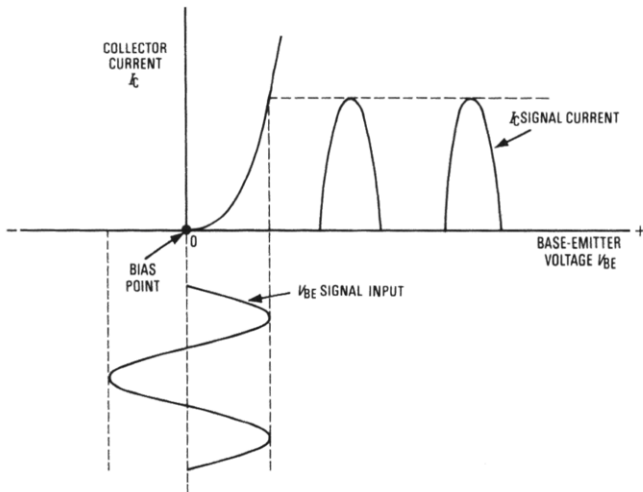
For Class C, the bias is below the cut-off point so that the angle of flow is less than 180° . The actual value depends on the bias chosen—the further it is beyond the cut-off point, the smaller is the angle of flow.

(b) Class A bias is used where linear amplification is required such as for audio-frequency voltage amplifiers or power amplifiers. The latter may be single-ended or push-pull types.



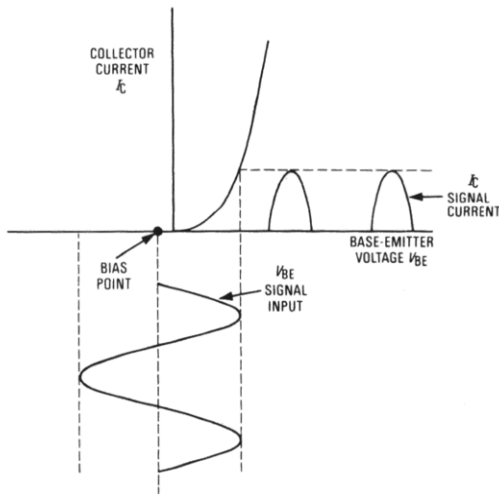
CLASS A BIAS

(a)



CLASS B BIAS

(b)



CLASS C BIAS

(c)

Class B bias severely distorts the signal since one half cycle is cut off. Class B can be used therefore only in circuit arrangements which restore the missing half cycle. Examples are audio-frequency Class B push-pull power amplifiers, where two transistors are used each producing one half cycle which are joined to form a complete cycle; and Class B radio-frequency amplifiers in which tuned circuits restore a complete cycle.

Class C bias is used in Class C radio-frequency amplifiers or oscillator circuits where tuned circuits restore the complete cycles from the output current pulses.

(c) Class A bias is used where linear amplification is required. A disadvantage in power amplifier circuits is low efficiency, which has a maximum theoretical value of 50%.

Class B bias is used to obtain higher efficiency, the maximum theoretical value being 78.5%. A disadvantage in push-pull audio-frequency amplifier circuits is distortion due to the lower bend in the characteristic.

Class C bias is used in radio-frequency power amplifiers where possible because it has even greater efficiency than Class B.

Q4 (a) Define

- (i) signal-to-noise ratio, and
- (ii) noise factor of an amplifier or receiver.

(b) A receiver has a noise factor of 15 dB. A signal with a signal-to-noise ratio of 40 dB is applied to its input. Determine

- (i) the signal-to-noise ratio in the output load of the receiver, and
- (ii) the noise power in the output load if the signal power developed in it is 2 W.

(c) State THREE possible sources of noise which originate in a receiver and the precautions which may be taken to minimise the noise level from these sources.

A4 (a) (i) The output of a communication system, for example, a radio system, line system or an amplifier, contains unwanted voltages apart from the wanted signal components. These unwanted components, known as noise, are generated by both active and passive components in the system as well as by external sources.

The signal-to-noise ratio is expressed as the ratio

$$\frac{\text{wanted signal power } (P_S)}{\text{unwanted noise power } (P_N)}$$

It is usual to express this ratio in decibels:

$$\text{signal-to-noise ratio} = 10 \log_{10} \frac{P_S}{P_N} \text{ dB, or}$$

$$\text{signal-to-noise ratio} = 20 \log_{10} \frac{V_S}{V_N} \text{ dB,}$$

where V_S and V_N are RMS values of signal and noise, respectively.

(ii) The input signal to a system is seldom entirely 'clean'; that is, it contains a noise component. The output of the system has a different signal-to-noise ratio depending upon its noise characteristics.

The noise factor, F ,

$$= \frac{\text{input signal-to-noise power ratio}}{\text{output signal-to-noise power ratio}}$$

This is also expressed in decibels:

$$F = 10 \log_{10} \frac{\text{input signal-to-noise power ratio}}{\text{output signal-to-noise power ratio}}$$

(b) (i)

$$15 = 10 \log_{10} \frac{\text{input signal-to-noise power ratio}}{\text{output signal-to-noise power ratio}}$$

$$\text{Antilog}_{10} 1.5 = \frac{\text{input signal-to-noise power ratio}}{\text{output signal-to-noise power ratio}} = 31.6. \quad \dots (1)$$

Input signal-to-noise power ratio = 40 dB.

$$\therefore 10 \log_{10} (\text{input signal-to-noise power ratio}) = 40.$$

$$\therefore \text{input signal-to-noise power ratio} = \text{antilog}_{10} 4 = 10^4. \quad \dots (2)$$

From equations (1) and (2),

$$\begin{aligned} \text{output signal-to-noise ratio} &= \frac{10^4}{31.6} = 316, \\ &= 10 \log_{10} 316 \text{ dB}, \\ &= 25 \text{ dB}. \end{aligned}$$

$$\begin{aligned} (ii) \quad 316 &= \frac{\text{signal power in load}}{\text{noise power in load}}, \\ &= \frac{2 \text{ W}}{\text{noise power in load}}. \end{aligned}$$

\therefore noise power in load

$$= \frac{2}{316} \text{ W} = 6.3 \text{ mW}.$$

- (c) Some possible sources of noise that may originate in a receiver are
- thermal noise in resistive components,
 - shot noise in transistors,
 - partition noise in transistors,
 - transistor $1/f$ noise,
 - hum, and
 - intermodulation effects.

Design factors which should be considered to minimise noise are as follows:

- The bandwidth should be restricted to that needed for signal transmission. This is because most forms of noise have an equal energy distribution per unit bandwidth over the frequency spectrum (known as white noise).
- Thermal noise is a function of resistance value; high resistance values should therefore be avoided, particularly in the early stages of a system.
- Thermal noise increases with temperature; design should be aimed at minimising the rise in temperature of components in sensitive parts of the circuit.
- Low-noise transistors should be used in sensitive parts of the circuit. Field-effect transistors (FETs) have inherently lower shot noise and partition noise than bipolar devices.
- Attention should be paid to circuit design in terms of power supply smoothing (to minimise hum), linearity of device characteristics (to minimise intermodulation effects), bandwidth of tuned circuits (to reject unwanted signals) and the use of screening (to avoid coupling between sections of the circuit).

Q5 (a) Explain the effects of applying voltage-derived negative feedback in series with the input to an amplifier upon

- voltage gain
- voltage gain stability
- bandwidth
- input impedance
- output impedance.

(b) With reference to Fig. 2, if the voltage gain A of the amplifier without feedback is 1200, determine

- the value of the feedback fraction
- the voltage gain V_{out}/V_{in} of the amplifier with feedback.

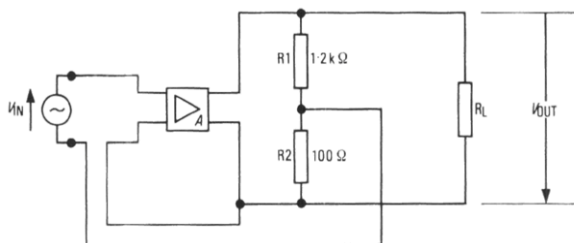


Fig. 2

A5 (a) (i) The gain of an amplifier with negative feedback, A' , is given by

$$A' = \frac{A}{1 + A\beta} \quad \dots\dots (1)$$

where A is the voltage gain of the amplifier without feedback, and β is the feedback fraction.

Clearly, from equation (1), A' must be less than A .

(ii) In most practical cases, $A\beta \gg 1$. Therefore, from equation (1),

$$A' \approx \frac{A}{A\beta} = \frac{1}{\beta}$$

Thus, A' is independent of A within the limitations of the approximation. This means that changes in A due to variations in supply voltage, temperature effects, ageing of components, etc. do not affect A' to a great extent.

(iii) The bandwidth of the amplifier with negative feedback is greater than that of the amplifier itself. This may be regarded as a consequential effect of (ii) wherein the fall in A caused by a change in frequency has little effect upon the value of A' . It can be shown that

$$f'_{oh} = f_{oh}(1 + A\beta), \quad \text{and}$$

$$f'_{ol} = \frac{f_{ol}}{1 + A\beta},$$

where f_{oh} is the high-frequency cut-off frequency without negative feedback,

f'_{oh} is the high-frequency cut-off frequency with negative feedback, f_{ol} is the low-frequency cut-off frequency without negative feedback, and f'_{ol} is the low-frequency cut-off frequency with negative feedback.

Thus, $f'_{oh} > f_{oh}$, and $f'_{ol} < f_{ol}$.

(iv) The application of negative feedback in series with an amplifier increases the input impedance. This is because the voltage across the amplifier input terminals is reduced by the feedback voltage, so that the input current to the amplifier is reduced.

(v) Voltage-derived negative feedback produces an output impedance less than that of the amplifier itself. It can be shown that the output impedance of the amplifier with voltage-derived feedback, R'_o , is given by

$$R'_o = \frac{R_o}{1 + A_o\beta},$$

where R_o is the output impedance of the amplifier without negative feedback (assumed resistive), and A_o is the open-circuit gain of the amplifier without negative feedback.

(b) (i) From the circuit given,

$$\beta = \frac{100}{1200 + 100} = \frac{1}{13} = 0.077.$$

(ii) From equation (1),

$$A' = \frac{1200}{1 + 0.077 \times 1200} = \frac{1200}{93.4} = 12.85.$$

[Tutorial Note: Alternatively, $A' \approx 1/\beta$, $1/0.077 = 13$.]

Q6 (a) State the conditions which must be satisfied to maintain oscillations in an oscillator at a particular frequency.

(b) Draw the circuit diagram for ONE type of L-C oscillator.

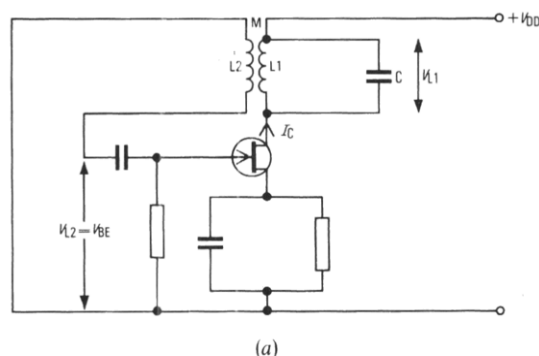
(c) For the oscillator given in (b)

- explain how the conditions for oscillation are satisfied, and
- state the circuit parameters upon which the frequency of oscillation mainly depends.

A6 (a) The two conditions for oscillation at a particular frequency in an oscillator circuit are that at that frequency

- the magnitude of the loop gain must be at least equal to unity, and
- the loop-gain phase shift must be zero (or a multiple of 360°).

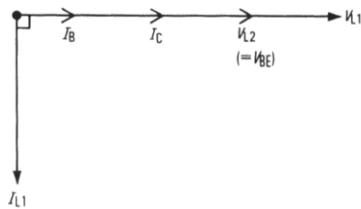
(b) See sketch (a).



[Tutorial Note: There are many forms of L-C oscillator; the circuit shown is a tuned-drain type. By transferring capacitor C to across inductor $L2$, it becomes a tuned-gate type. Similar tuned-collector or tuned-base forms can be constructed by using a bipolar transistor in place of the field-effect transistor (FET). Other well-known L-C oscillators are the Hartley and the Colpitts oscillators.]

(c) (i) The condition for zero loop phase shift is met as follows. Starting from V_{BE} , I_B and therefore I_C are in phase with it. At the resonant frequency, the parallel tuned circuit formed by inductor $L1$ and capacitor C has a resistive impedance, so that the voltage across it, V_{L1} , is in phase with I_C . The current in inductor $L1$ lags this voltage by 90° (neglecting resistance in the inductor). But the voltage induced in the secondary, $L2$, by I_{L1} is 90° out of phase with it, and this brings V_{L2} in phase with V_{L1} and therefore with V_{BE} . Thus, the loop phase shift is zero. See sketch (b).

The condition for the magnitude of the loop gain to be at least unity requires the amplification of the stage to compensate for the attenuation around the feedback loop which is due mainly to the mutual coupling effect between the two coils. It can be shown that for this condition to be met, assuming that the resistance of inductor $L1$ is negligible, the mutual inductance, M , meets the condition



(b)

$$M \geq \frac{L_1}{g_m r_{ds}} \text{ henries,}$$

where g_m is the mutual conductance, and r_{ds} is the drain slope resistance of the FET.

(ii) The frequency of oscillation, f_o , is at the resonant frequency of the tuned circuit and therefore depends upon L_1 and C :

$$f_o \approx \frac{1}{2\pi\sqrt{L_1 C}} \text{ hertz.}$$

It will be noted that this is an approximation because other parameters in the circuit, particularly the resistance of the inductor L_1 , affect the loop phase shift.

Q7 (a) For a non-sinusoidal oscillator, explain and give an application of the following:

- (i) synchronisation, and
- (ii) triggering.

(b) With the use of input and output waveform diagrams, compare the operation of

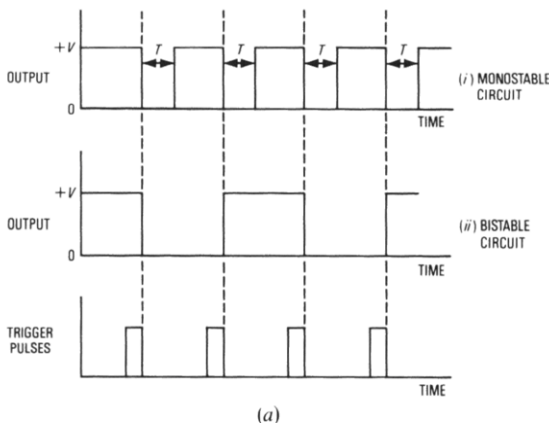
- (i) a monostable,
- (ii) a bistable, and
- (iii) a Schmitt trigger.

A7 (a) (i) Often the particular application of a non-sinusoidal oscillator demands a very precise value of frequency without drift. A free-running circuit cannot easily meet these demands. Controls are not sufficiently fine to set the frequency to a precise value and, even if this was possible, drift due to temperature and voltage variations, for example, would soon alter the value. The problem can be overcome by the application of synchronising pulses which 'lock' the oscillator frequency to the desired value. The synchronising pulses can be obtained from an accurate timing source, such as a quartz crystal, or from a signal to which the oscillator frequency has to be related. An example of the latter is in a cathode-ray oscilloscope, where the signal to be displayed is used to synchronise the time-base oscillator.

Another example is the use of quartz-controlled master oscillators to lock the frequency of timing circuits.

(ii) Triggering is a term used to describe the action of pulses (called trigger pulses) when they are used to change the state of a circuit at a particular instant. Examples are the triggering of a bistable circuit to cause it to change state, and triggering of a monostable circuit to switch it to the quasi-stable state.

(b) See sketch (a).



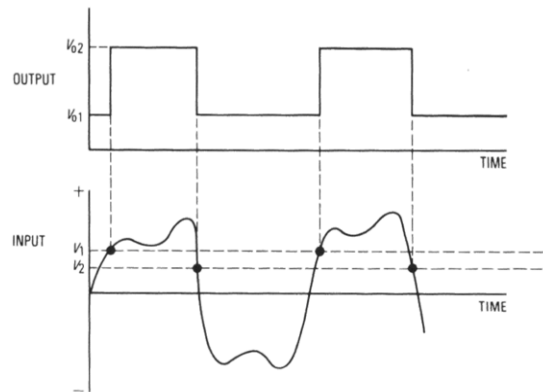
(a)

(i) Sketch (a) shows the output of a monostable circuit. In the stable state, the output level (for example, one of the collector voltages) is assumed to be V volts. The trigger causes the circuit to switch to the quasi-stable state, in which the output is assumed to be 0 volts. The circuit remains in this state for T seconds, depending on the values of the monostable C-R timing

components, and then switches back to the stable condition, in which it remains until the next trigger pulse is applied. (It is assumed that the trigger initiates on the lagging edge of the trigger pulse.)

(ii) The bistable circuit (see sketch (a)) has a different action because it changes state when a trigger pulse is applied and remains in this changed state until the next trigger pulse is applied.

(iii) See sketch (b).



(b)

The Schmitt trigger is a circuit in which the output is at a certain level (V_{01}) when the input is at zero. If the input is raised to a certain critical value (V_1), the output switches with a fast rise time to another level (V_{02}). Increasing the input beyond V_1 maintains this state, but, if it is reduced to another critical value (V_2), the output level switches rapidly back to V_{01} . The difference between V_1 and V_2 is known as the circuit *backlash*. The circuit thus produces a rectangular output waveform with fast rise and fall times from an input waveform of arbitrary shape, provided that the amplitude of the input signal is large enough to cause a trigger.

Q8 (a) State

- (i) the meaning of a 'linear integrated circuit', and
- (ii) two advantages and two disadvantages of a circuit of the type in (i) compared with a similar circuit using discrete components.

(b) For an operational amplifier,

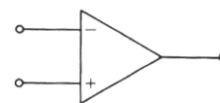
- (i) draw the circuit symbol,
- (ii) explain its basic operation, and
- (iii) list the ideal properties.

(c) Give a circuit diagram to show an application of an operational amplifier and describe the function of the circuit.

A8 (a) (i) An integrated circuit is a complete and often complex electronic circuit which is formed on a semiconductor chip, usually of silicon. A digital integrated circuit is one in which input and output signals have one of two possible levels (one is usually defined as logic 0, and the other logic 1). In contrast, signals for linear integrated circuits take the form of continuously varying voltages (except for some special applications when they are operated in the saturated mode). Linear amplification takes place between input and output signals.

(ii) Advantages of engineering a linear electronic circuit as an integrated circuit compared to discrete form are smaller size, lower costs (provided that sufficient numbers are to be produced to offset high initial design and development costs), small power consumption and generally better reliability, together with advantages in servicing and advantages in circuit design and performance which arise from the compact homogeneous environment in which the circuit elements exist. Disadvantages are limited power output capability and susceptibility to damage because of electrical or mechanical misuse.

(b) (i)



(ii) The '-' terminal is known as the *inverting input* and the '+' terminal as the *non-inverting input*. When a signal is applied to the '-' input, it produces an amplified output with a 180° phase inversion, whereas a signal applied to the '+' terminal produces an amplified in-phase output. If in-phase signals of equal magnitude are applied to the two inputs, the output

is, theoretically, at zero (such inputs are called *common-mode* inputs). If antiphase signals are applied to the two inputs, there is a large output since the inversion of the '−' input signal brings the two output components into phase with each other (such inputs are known as *differential-mode* inputs). An advantage of the arrangement is that output drift is minimised because factors such as temperature and supply voltage changes, which cause drift in the output of high-gain DC amplifiers, have common-mode effects.

(iii) An operational amplifier is a high-gain amplifier which is normally used with negative feedback. Theoretically, if the gain of the amplifier is infinite, then the characteristics of the overall system are independent of the amplifier and dependent upon external feedback circuitry. Thus, the amplifier can perform operations dependent upon this external circuitry and consequently has many operational applications. To behave in the manner described above, an operational amplifier should ideally have infinite gain, infinite input impedance, zero output impedance, a bandwidth from DC to infinity and zero drift.

(c) [Tutorial Note: There are many applications of operational amplifiers which can be referred to in appropriate texts.]

Q9 (a) For an *n*-type depletion mode MOS field-effect transistor (MOSFET), with the aid of a suitable diagram, describe its fundamental operating principles.

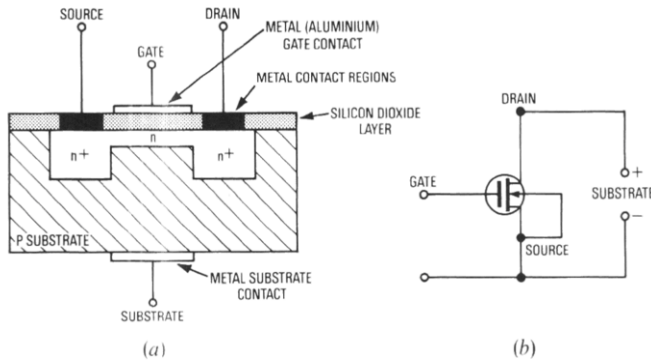
(b) Sketch and label a typical family of drain characteristics for the device in (a).

(c) Using the characteristics in (b) show how

- the drain slope resistance (r_{ds}), and
- the mutual conductance (g_m)

may be obtained. State typical values for these parameters.

A9 (a)



Sketch (a) shows an *n*-channel *p*-substrate depletion-type MOSFET construction and sketch (b) its symbol, together with the drain–source bias polarity. Note that the drain region must be reverse biased with respect to the substrate to prevent forward current flow between the two regions. This is normally achieved by connecting the substrate to the source.

With zero gate voltage, current can flow between the heavily doped *n*⁺ drain and source regions via the *n* channel. The current depends upon the channel resistance and, as the drain–source voltage is increased from zero, I_D at first rises linearly, but a value is reached at which pinch-off occurs. Beyond this, the rate of increase with V_{DS} is small. Pinch-off occurs because the channel is reverse biased with respect to the adjacent *p* substrate region and there is a depletion spread into the channel (a region with no majority carriers and consequently very high resistance). The spread increases with the value of V_{DS} until the channel is eventually pinched-off.

If a negative voltage is applied between gate and source/substrate, electron carriers are repelled from the *n* channel, its resistivity increases and I_D falls. This is known as *depletion-mode operation*.

Although the device is a depletion-mode type, it can be operated in enhancement mode. This is achieved by applying a positive gate voltage which attracts minority carriers (*n* type) from the *p* substrate to the channel region; thereby the carrier concentration is enhanced which reduces resistivity so that I_D increases.

Note that, with MOSFETs, the gate is insulated from the *n*-channel region by the high-resistivity silicon dioxide layer. Hence, the gate input resistance is extremely high, and may be as high as 10^4 MΩ.

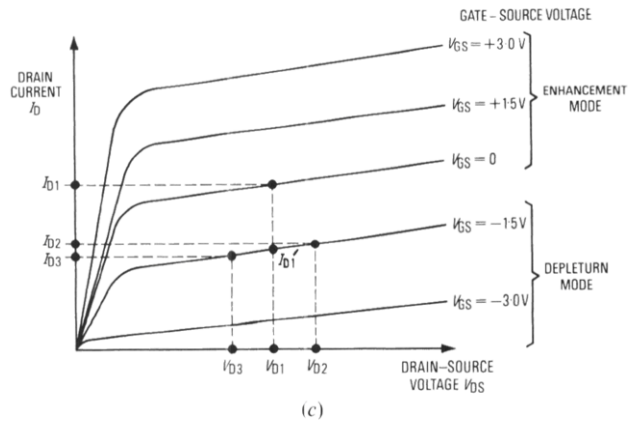
(b) See sketch (c).

(c) (i) Drain slope resistance, r_{ds} , is defined as

$$\frac{\Delta V_{DS}}{\Delta I_D} \quad (V_{GS} \text{ constant}) \text{ ohms,}$$

where ΔV_{DS} is a small change in voltage V_{DS} , and ΔI_D a small change in current I_D .

Thus, from the characteristics



$$r_{ds} = \frac{V_{D2} - V_{D3}}{I_{D2} - I_{D3}} \quad (V_{GS} \text{ constant at } -1.5 \text{ V}).$$

Typically, values of r_{ds} are in the range 10 kΩ–100 kΩ.

(ii) Mutual conductance (g_m) is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ mA/V} \quad (V_{DS} \text{ constant}).$$

[Tutorial Note: Units can alternatively be expressed in siemens (S).]

From the characteristics,

$$g_m = \frac{I_{D1} - I_{D1}}{0 - (-1.5)} \quad (V_{DS} \text{ constant at } V_{D1} \text{ volts}).$$

Typical values are in the range 2 mA/V–15 mA/V.

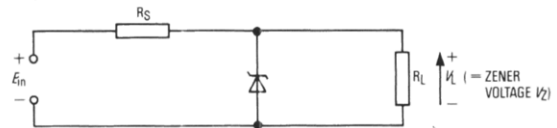
Q10 (a) Draw

(i) a circuit diagram for a simple Zener-diode stabiliser, and
(ii) a block diagram for a series stabilised power supply using the comparator technique.

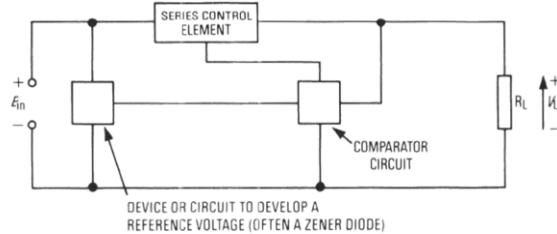
(b) For the series stabilised power supply in (a) (ii)

- explain its operation, and
- compare its performance with that of the simple Zener-diode stabiliser.

A10 (a) (i)



(ii)



(b) (i) The principle of circuit (a) (ii) is that the voltage across the load (V_L) is compared against a fixed reference voltage in such a way that changes in the difference between them generate an output to the series control element. This output increases or decreases the effective series resistance of the control element so as to restore the difference between V_L and the reference to its original value.

(ii) Compared with the simple Zener-diode stabiliser circuit, the comparator permits a greater range of load current. In the case of the Zener-diode circuit, the I_L range is limited to that of the Zener diode, whereas, for the comparator circuit, it depends on the series control element (usually a transistor). Furthermore, the comparator method has a better stabilisation ratio. This is because the changes in the difference between V_L and the reference voltage are amplified before application to the series element, which leads to a very sensitive control.

Finally, for the simple Zener-diode circuit, the load voltage is equal to V_Z since they are in parallel. This restriction does not present itself in the comparator circuit.

Answers contributed by E. T. Fleury

Students were required to answer any six questions. The time allowed was three hours. Students are advised to read the notes on p. 41

Q1 (a) (i) State Kirchhoff's laws.

(ii) State Thévenin's theorem.

(b) Use either of the theorems in (a) to calculate the current in the $20\ \Omega$ resistor in the network of Fig. 1. State clearly each step in the calculation.

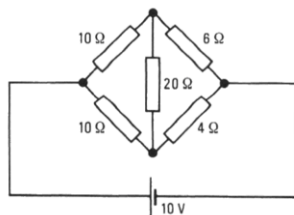


Fig. 1

Q2 (a) When 6 V DC is applied across an inductor, the current is 80 mA. When the supply is changed to 12 V 50 Hz, the current is 50 mA RMS. Find the inductance and DC resistance of the inductor.

(b) A capacitor is connected in series with the inductor in (a). When the frequency of the supply is varied, the voltage being held constant, the current is found to be a maximum at 9.2 kHz.

(i) Explain why the current alters with frequency.

(ii) Explain why there is a maximum value for the current.

(iii) Calculate the value of the capacitor.

A2 (a) With a DC voltage of 6 V applied across the inductor, the current of 80 mA is attributable to the DC resistance, if steady-state conditions are assumed.

$$\begin{aligned} \text{DC resistance, } R &= \frac{V}{I} \\ &= \frac{6}{0.08} \\ &= 75\ \Omega. \end{aligned}$$

With an AC supply of 12 V 50 Hz, the current is 50 mA RMS.

$$\begin{aligned} \text{Impedance, } Z &= \frac{V}{I} \\ &= \frac{12}{0.05} \\ &= 240\ \Omega. \end{aligned}$$

But, at frequency f , $Z = \sqrt{R^2 + X_L^2}$, where $X_L = 2\pi fL$.

$$\therefore 240 = \sqrt{75^2 + (2\pi \times 50L)^2}.$$

$$\therefore 240^2 = 75^2 + 4\pi^2 \times 2500L^2.$$

$$\therefore L^2 = \frac{240^2 - 75^2}{4\pi^2 \times 2500},$$

$$= \frac{57\ 600 - 5625}{4 \times 9.872 \times 2500},$$

$$= \frac{51\ 975}{98\ 720},$$

$$= 0.5265.$$

$$\therefore L = 0.726\ \text{H}.$$

Therefore, the inductance = 0.726 H with a DC resistance of 75 Ω .

(b) (i) With a capacitor connected in series with the inductor, when the frequency of the supply is varied with the voltage held constant, the current varies with frequency. This is because the impedance of the circuit, Z , given by the expression $R + j\left(\omega L - \frac{1}{\omega C}\right)$ ($\omega = 2\pi \times \text{frequency}$) varies with frequency, and $I = \frac{V}{Z}$.

(ii) A maximum value for the current occurs when the impedance, Z , is a minimum (since $I = \frac{V}{Z}$ and V is held constant).

The value of $\omega L - \frac{1}{\omega C}$ varies with frequency; at low values of frequency,

the capacitance has a high reactance ($X_C = \frac{1}{\omega C}$) whereas, at high values of frequency, the inductance has a high reactance ($X_L = \omega L$). When $X_C = X_L$, the reactive terms in the impedance expression cancel each other out and $Z = R$.

(iii) At resonance, $X_L = X_C$,

$$\text{and } \omega L = \frac{1}{\omega C}.$$

Rearranging the expression gives

$$\begin{aligned} C &= \frac{1}{\omega^2 L}, \\ &= \frac{1}{(2\pi \times 9.2 \times 10^3)^2 \times 0.726}, \\ &= \frac{1}{4\pi^2 \times 9.2^2 \times 10^6 \times 0.726}, \\ &= \frac{10^{-6}}{4 \times 9.872 \times 84.64 \times 0.726}, \\ &= \frac{10^{-6}}{2426.5}, \\ &= 412.1 \times 10^{-12}, \\ &= 412\ \text{pF}. \end{aligned}$$

Q3 (a) Explain the meaning of impedance and show how it is represented graphically.

(b) An inductance of 0.4 H and 200 Ω resistance is connected in series with a capacitor of 0.9 μF .

If the circuit current is 15 mA at 500 Hz,

(i) draw a phasor diagram to scale relating the voltages and the supply current;

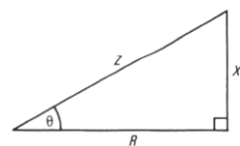
(ii) find the impedance of the circuit and the phase angle;

(iii) calculate the power factor; and

(iv) find the power taken by the circuit from the supply.

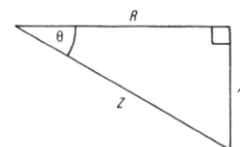
A3 (a) Impedance is the ratio of the RMS EMF applied to a circuit to the RMS current which the circuit takes. Impedance is the vector sum of the resistance and reactance in a circuit and this can be represented graphically by the impedance triangle.

In sketch (a), an impedance triangle is formed for an inductance in series with a resistor. The two sides at right-angles to one another represent the resistance R (horizontal) and the reactance X_L (vertical), and completion of the third side gives the impedance Z .



(a)

In sketch (b), an impedance triangle is formed for a capacitor in series with a resistor. The two sides at right-angles to one another represent the resistance R (horizontal) and the reactance X_C (vertical), and completion of the third side gives the impedance Z .

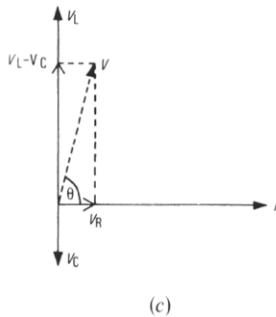


(b)

(b) For the series circuit, the voltages across the components, V_R , V_L and V_C , are calculated as follows:

$$\begin{aligned}
 V_R &= IR, \\
 &= 0.015 \times 200, \\
 &= 3 \text{ V}, \\
 V_L &= I \times 2\pi fL \quad (f = \text{frequency}), \\
 &= 0.015 \times 2\pi \times 500 \times 0.4, \\
 &= 18.85 \text{ V}, \\
 V_C &= \frac{I}{2\pi fC}, \\
 &= \frac{0.015}{2\pi \times 500 \times 0.9 \times 10^{-6}}, \\
 &= 5.3 \text{ V}.
 \end{aligned}$$

(i) A phasor diagram relating the voltages and the supply current is given in sketch (c).



(ii) To find the impedance of the circuit, as the voltages have already been obtained to draw the phasor diagram,

$$\begin{aligned}
 V &= \sqrt{V_R^2 + (V_L - V_C)^2}, \\
 &= \sqrt{3^2 + (18.85 - 5.3)^2}, \\
 &= \sqrt{3^2 + 13.55^2}, \\
 &= \sqrt{9 + 183.6}, \\
 &= 13.88 \text{ V}.
 \end{aligned}$$

$$\begin{aligned}
 \text{Now, } Z &= \frac{V}{I}, \\
 &= \frac{13.88}{0.015}, \\
 &= 925.2 \Omega.
 \end{aligned}$$

$$\begin{aligned}
 \text{The phase angle, } \theta &= \tan^{-1} \frac{13.55}{3}, \\
 &= \tan^{-1} 4.517, \\
 &= 77^\circ 30'.
 \end{aligned}$$

$$\text{Impedance} = 925.2 \angle 77^\circ 30' \Omega.$$

$$\begin{aligned}
 \text{(iii) Power factor} &= \cos \theta, \\
 &= \frac{3}{13.88}, \\
 &= 0.216.
 \end{aligned}$$

$$\begin{aligned}
 \text{(iv) The power taken from the supply} \\
 &= V \times I \times \text{power factor}, \\
 &= 13.88 \times 0.015 \times 0.216, \\
 &= 0.045, \\
 &= 45 \text{ mW}.
 \end{aligned}$$

- Q4** (a) Define the decibel and explain why it is used in telecommunications.
 (b) Give the meanings of dBm and dBW.
 (c) An amplifier of input resistance $12 \text{ k}\Omega$ feeds a loudspeaker of

impedance 8Ω . When the amplifier input is 250 mV the loudspeaker receives 10 W . Calculate the power gain of the amplifier in decibels.

A4 (a) The decibel is defined as

$$10 \log_{10} \left(\frac{P_{\text{OUT}}}{P_{\text{IN}}} \right),$$

where P_{IN} is the power applied to a network or system and P_{OUT} is the power at the output.

The decibel is used in telecommunications because, normally, power ratios can result in large numbers, and, to determine the overall power ratio of a system or network, could entail multiplying cumbersome figures. By taking the logarithms of the power ratios, evaluation of the overall power ratio can be found in terms of a logarithmic quantity by simply taking the algebraic sum of the separate logarithmic power ratios.

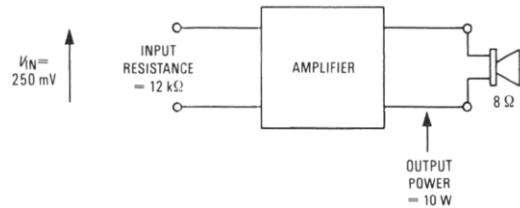
(b) The term 'dBm' is an indication of a power ratio which compares a given power level with a reference power level of 1 mW ; that is,

$$\text{power in dBm} = 10 \log_{10} \left(\frac{\text{measured power in milliwatts}}{1} \right).$$

The term 'dBW' is an indication of a power ratio which compares a given power level with a reference power level of 1 W ; that is,

$$\text{power in dBW} = 10 \log_{10} \left(\frac{\text{measured power in watts}}{1} \right).$$

(c) The sketch shows the amplifier.



$$\begin{aligned}
 \text{The input power} &= \frac{V^2}{R}, \\
 &= \frac{(0.25)^2}{12 \times 10^3}, \\
 &= 5.2 \mu\text{W}.
 \end{aligned}$$

$$\begin{aligned}
 \text{Power gain of amplifier} &= 10 \log_{10} \frac{P_{\text{OUT}}}{P_{\text{IN}}}, \\
 &= 10 \log_{10} \frac{10}{5.2 \times 10^{-6}}, \\
 &= 10 \log_{10} (1.923 \times 10^6), \\
 &= 10 \times 5.284, \\
 &= 52.84 \text{ dB}.
 \end{aligned}$$

Q5 With reference to the circuit in Fig. 2.

(a) Explain

(i) what is meant by the time constant of the circuit, and
 (ii) why the current in the coil takes time to build up to a steady value when the switch S is closed to position (p).

(b) (i) Give an expression relating the current in the coil to the time from closing the switch.

(ii) Sketch the curve relating the coil current and time from the instant of connection. Label the axes.

(iii) Find the initial coil current.

(iv) Calculate the power taken when the current reaches its steady value.

(c) (i) Give the expression relating the coil current and time from the opening of the switch to position (q).

(ii) Sketch this curve and find the new time constant.

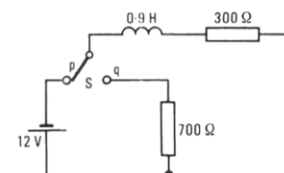


Fig. 2

A5 (a) (i) The time constant in a resistance-inductance circuit is the ratio L/R . Expressed in seconds, L/R is the time that the current takes to reach 63% of its steady-state value when a DC voltage is applied. The current reaches its steady-state value in $5 \times L/R$ seconds.

(ii) At the instant that the switch is closed to position p, a back EMF is generated in the inductor L , equal but opposite to the applied voltage. At this instant, the current is zero. Subsequently the back EMF reduces in value as the current i grows from zero; in the steady-state the current $i = \frac{V}{R}$, and inductor L acts effectively as a short circuit.

(b) (i) The current flowing in the coil after time t is given by the expression

$$i = I\{1 - e^{-t/(L/R)}\},$$

where $I = \frac{V}{R}$, the steady-state current due to a DC source of voltage V .

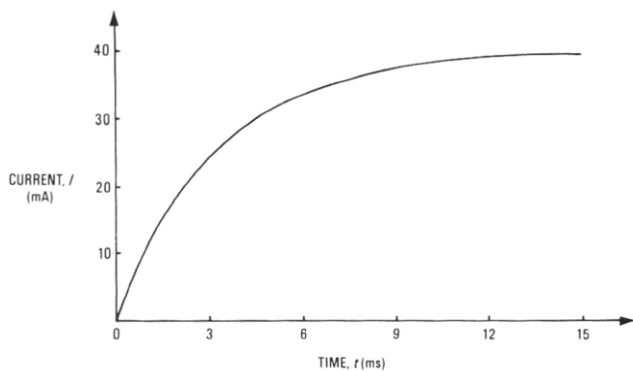
(ii) For the circuit with the switch in position p,

$$\begin{aligned} I &= \frac{V}{R}, \\ &= \frac{12}{300}, \\ &= 40 \text{ mA}. \end{aligned}$$

The time constant,

$$\begin{aligned} \frac{L}{R} &= \frac{0.9}{300}, \\ &= 3 \text{ ms}. \end{aligned}$$

Sketch (a) indicates how the coil current varies with time from the instant of connection of the switch to position p.



(a)

(iii) The initial coil current is zero.

(iv) Power taken when the current reaches its steady value, P

$$\begin{aligned} &= \frac{V^2}{R}, \\ &= \frac{12^2}{300}, \\ &= 0.48 \text{ W}. \end{aligned}$$

(c) (i) The current flowing in the coil is given by the expression

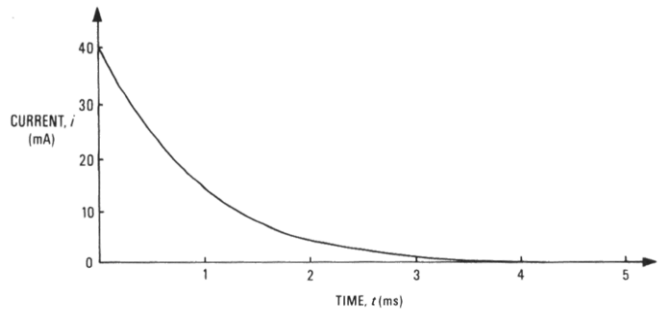
$$i = I e^{-t/(L/R)}$$

where I is the steady-state current immediately before the switch is moved to position q and R is the new circuit resistance.

(ii) The new time constant, L/R ,

$$\begin{aligned} &= \frac{0.9}{300 + 700}, \\ &= 0.9 \text{ ms}. \end{aligned}$$

Sketch (b) indicates how the coil current varies with time from when the switch is opened to position q.



(b)

Q6 (a) A transformer is to be used to match a 75Ω 100 V AC source to a 225Ω load. The transformer is wound at the rate of two turns per volt. Calculate

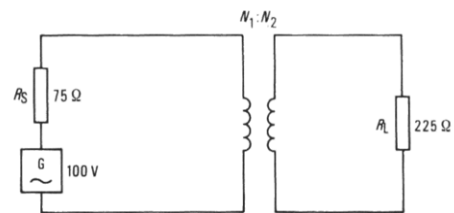
- the number of primary turns,
- the ratio of the primary to secondary turns, and
- the power taken from the supply, assuming the transformer is ideal.

(b) State two sources of loss that would occur in a practical transformer.

(c) Explain briefly how the magnitude of each type of loss in (b) is related to

- the load current, and
- the frequency of the supply.

A6 (a) Sketch (a) indicates the circuit arrangements.



(a)

(i) If the transformer is wound at the rate of two turns per volt, and the primary voltage is 100 V , then the number of primary turns,

$$N_1 = 2 \times 100 = 200.$$

(ii) For matching, where R_S is the source resistance and R_L the load resistance,

$$R_S = \left(\frac{N_1}{N_2}\right)^2 R_L.$$

Rearranging the equation for N_2 gives

$$\begin{aligned} \left(\frac{N_1}{N_2}\right)^2 &= \frac{R_S}{R_L}, \\ \therefore \frac{N_1}{N_2} &= \sqrt{\left(\frac{R_S}{R_L}\right)}, \\ N_2 &= \frac{N_1}{\sqrt{\left(\frac{R_S}{R_L}\right)}}. \end{aligned}$$

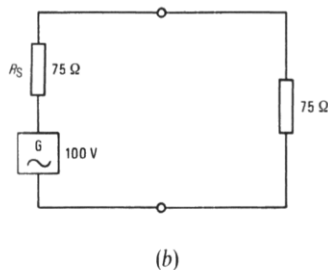
Substituting given values gives

$$\begin{aligned} N_2 &= \frac{200}{\sqrt{\left(\frac{75}{225}\right)}}, \\ &= \frac{200}{\sqrt{\left(\frac{1}{3}\right)}}, \\ &= \frac{200}{0.5774}, \\ &= 346.4. \end{aligned}$$

(iii) When the transformer matches the load to the source, the source

impedance equals the value of the load impedance as reflected through the transformer.

The equivalent circuit is given in sketch (b).



Power taken from the supply

$$\begin{aligned}
 &= \frac{V^2}{R}, \\
 &= \frac{100^2}{150}, \\
 &= 66\frac{2}{3} \text{ W.}
 \end{aligned}$$

(b) There are two principal causes of loss in a transformer: iron losses, consisting of hysteresis and eddy-current losses; and copper losses, which are the resistance losses occurring in the primary and secondary windings.

(c) For the iron losses, hysteresis loss is directly proportional to the frequency of the supply, and eddy-current loss is directly proportional to the square of the frequency of the supply. Iron losses are largely independent of the load current.

Copper losses are directly proportional to the square of the current; they are independent of the frequency of the supply.

Q7 (a) State the purpose and application of a DC face-plate starter. Sketch and describe the action of a typical face-plate starter with no-volt and overload protection devices.

(b) Explain why it is better to control the speed of a DC motor by adjusting the field current than by adjusting the armature current or the supply voltage.

Q8 (a) In a 3-phase delta-connected system of power distribution,

- (i) show that the line voltages are equal to the phase voltages; and
- (ii) find the relation between line current and phase current in a balanced system.

(b) A 3-phase motor giving an output power of 1.5 kW operates with a balanced input at 0.8 power factor. The line voltage is 415 V and the line current is 3.8 A. Calculate

- (i) the power input to the motor
- (ii) the efficiency of the motor.

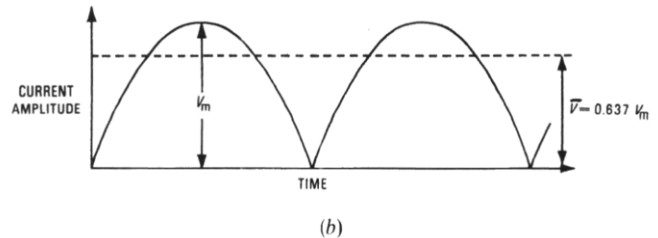
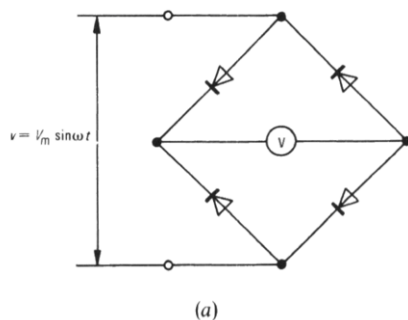
Q9 (a) Describe with the aid of a basic circuit the operation of a full-wave rectifier instrument for measuring audio-frequency voltage.

(b) Describe a method of calibrating the meter in (a).

(c) (i) Compare the readings given on the meter in (a) by a sine wave and a square wave of the same peak value.

(ii) Explain why there is a difference.

A9 (a) A bridge-rectifier AC voltmeter circuit is given in sketch (a). In this instrument, the main circuit voltage, as far as the meter is concerned, is rectified by the diode bridge, and the meter responds to the average of the full-wave rectified voltage as shown in sketch (b).



V_m = peak amplitude.

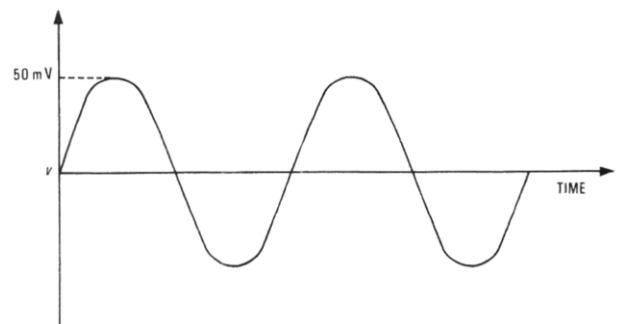
\bar{V} = average voltage flowing through the meter,

$$= \frac{2}{\pi} \times \text{peak value},$$

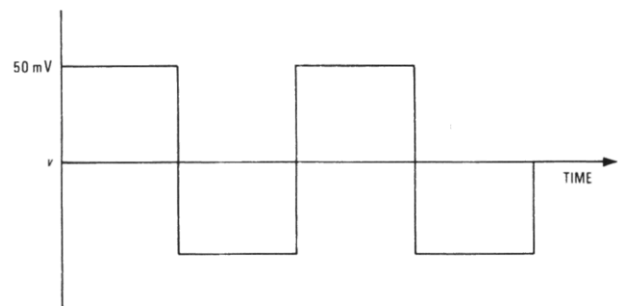
$$= 0.637 V_m.$$

(b) If the meter is to read RMS values directly, that is, $0.707 V_m$, a DC source can be used for calibration. Each DC reading must be scaled by $0.707 / 0.637 = 1.11$. If the value of the DC source is known, the meter can be calibrated for AC sources by using the scaling factor.

(c) (i) Sketch (c) shows a sine wave and a square wave having the same peak value.



(i) Sine wave



(ii) Square wave

(c)

For the sine wave of 50 mV peak, the meter reads $0.707 \times \text{peak value}$; that is, 35.4 mV. For the square wave of 50 mV peak, the meter reads $1.11 \times \text{peak value}$; that is, 55.5 mV.

(ii) The reason why there is a difference between the two readings is because the meter works on the full-wave rectified voltage and it is calibrated according to the expected response for alternating currents.

For the sine wave, the meter reads $0.707 \times 50 = 35.4$ mV. For the square wave, the rectified value of voltage is 50 mV, equivalent to a DC voltage of 50 mV. As the meter is calibrated to read AC voltages, the values include a scaling factor of 1.11, so the meter reads $1.11 \times 50 = 55.5$ mV.

Q10 (a) (i) Sketch and explain the construction of phasor diagrams relating voltages and currents in EACH of the circuits in Fig. 3 and Fig. 4.

(ii) Derive an expression for the phase angle of EACH of the circuits.

(b) Calculate the value of capacitance that will give the same phase angle for EACH of the circuits in Fig. 3 and Fig. 4, when $R_1 = 1 \text{ M}\Omega$, $R_2 = 0.01 \text{ M}\Omega$ and the frequency is 10 kHz.

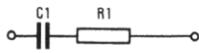


Fig. 3

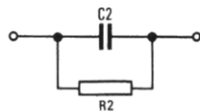
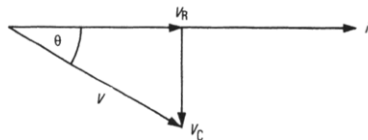


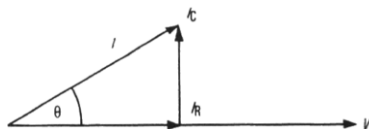
Fig. 4

A10 (a) (i) For the series resistor-capacitor combination, the phasor diagram is constructed by first determining the common parameter, either current to voltage, to which the other parameters can be related. In the case of the series circuit, the current is the common parameter. The voltage across the resistor, V_R , is in phase with the current. The current and the resistor voltage, V_R , are drawn horizontally. The voltage across the capacitor, V_C , is 90° out of phase with the current, since the current leads the voltage by 90° in a capacitor. The voltage across the capacitor, V_C , is drawn at 90° to the current and the resistor voltage, V_R , as shown in sketch (a). The voltage across the R-C combination, V , is obtained by completing the third side of the triangle as shown in sketch (a).



(a)

For the parallel resistor-capacitor combination, the phasor diagram is constructed by first determining the common parameter. For the parallel circuit, the voltage is the common parameter. The current through the resistor, I_R , is in phase with the voltage. Voltage V and current I_R are drawn horizontally, as shown in sketch (b). The current through the capacitor leads the voltage by 90° ; therefore, the capacitor current, I_C , is drawn at 90° to the voltage as shown in sketch (b). The total current, I , is obtained by completing the third side of the triangle.



(b)

(ii) For sketch (a),

$$\text{phase angle, } \theta = \tan^{-1} \left(\frac{V_C}{V_R} \right).$$

But,

$$V_C = iX_C = \frac{i}{\omega C_1},$$

and

$$V_R = iR_1,$$

where $\omega = 2\pi \times \text{frequency}$.

$$\therefore \frac{V_C}{V_R} = \frac{\frac{i}{\omega C_1}}{iR_1} = \frac{1}{\omega C_1 R_1}.$$

$$\therefore \theta = \tan^{-1} \left(\frac{1}{\omega C_1 R_1} \right).$$

For sketch (b),

$$\text{phase angle, } \theta = \tan^{-1} \frac{I_C}{I_R}.$$

But,

$$I_C = \frac{V}{X_C} = \frac{V}{\frac{1}{\omega C_2}} = V\omega C_2,$$

and

$$I_R = \frac{V}{R_2}.$$

$$\therefore \frac{I_C}{I_R} = \frac{V\omega C_2}{\frac{V}{R_2}} = \omega C_2 R_2.$$

$$\therefore \theta = \tan^{-1} \omega C_2 R_2.$$

(b) For the phase angles of the two circuits to be equal, it follows that the expressions derived in (a)(ii) will be equal; that is,

$$\tan^{-1} \left(\frac{1}{\omega C_1 R_1} \right) = \tan^{-1} \omega C_2 R_2,$$

when the phase angles are equal.

$$\therefore \frac{1}{\omega C_1 R_1} = \omega C_2 R_2.$$

Substituting given values gives

$$\frac{1}{2\pi \times 10^4 \times 10^6 C_1} = 2\pi \times 10^4 \times 10^4 C_2.$$

Rearranging,

$$C_1 C_2 = \frac{1}{4\pi^2 \times 10^{18}}.$$

But, if $C_1 = C_2$, then

$$C_1^2 = \frac{1}{4\pi^2 \times 10^{18}}.$$

$$\therefore C_1 = \frac{1}{2\pi \times 10^9} \text{ F},$$

$$= 159 \times 10^{-12} \text{ F},$$

$$= 159 \text{ pF}.$$

Answers contributed by J. Bush

CGLI: MICROELECTRONIC SYSTEMS T3 OPTION (1985)

Students were required to answer any six questions. The time allowed was three hours. Students are advised to read the notes on p. 41

Some parts of the questions involved the use of either of two sets of machine instruction sets and codes, attached as Tables 1 and 2 to the question paper. Because of insufficient space, these tables and the answers to the questions that require them have been omitted. However, the flow charts given are sufficiently detailed that the derivation of the solutions to these questions is relatively straightforward.

Q1 (a) Explain briefly what is meant by binary-coded decimal (BCD) representation of numbers.

(b) An 8 bit binary value represents two BCD digits. State the rules necessary in order to add two such 8 bit binary values and, if necessary, produce a corrected BCD sum.

(c) (i) Assuming BCD number representation, add EACH of the following

00110100 + 00100010
01110110 + 00010101
00101001 + 01010111

(ii) Convert the numbers into their decimal form to verify the results.

A1 (a) Binary-coded decimal (BCD) representation of numbers is a subset of the hexadecimal system. The output from a decimal (numeric) keypad is normally a 4 bit binary-coded value which represents a single decimal digit (0-9). Table 1 lists the 4 bit equivalent BCD codes of ten decimal digits.

Table 1

Decimal Digit	BCD Codes
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Since each decimal digit using BCD representation requires four bits, an 8 bit binary value stored within a microcomputer can represent two decimal digits; for example,

00111000 = 38 (decimal).

(b) Most arithmetic instructions within a microprocessor assume data is stored in their two's complement binary form. When BCD values are manipulated, it is necessary to perform some adjustments to the normal binary results in order to produce the correct results in the BCD form.

Assuming an 8 bit binary value represents two BCD digits, then, if the normal binary addition of each 4 bit group produces a result which is less than 9, and a carry is not produced when the two least significant BCD digits are added, then the result is correct.

If the result of the normal binary addition is greater than 9, or a carry is generated when the two least significant BCD digits are added, then a correction of +60110 must be added to the normal binary sum.

(c) (i) and (ii)

0 0 1 1 0 1 0 0 = BCD 34

0 0 1 0 0 0 1 0 = BCD 22

0 1 0 1 0 1 1 0 = BCD 56

Thus, no correction is necessary.

0 1 1 1 0 1 1 0 = BCD 76

0 0 0 1 0 1 0 1 = BCD 15

Incorrect value > 9 1 0 0 0 1 0 1 1 = BCD 8?

Add 6 correction 0 1 1 0 Correction necessary

1 0 0 1 0 0 0 1 = BCD 91

0 0 1 0 1 0 0 1 = BCD 29

0 1 0 1 0 1 1 1 = BCD 57

Incorrect carry 1 0 0 0 0 0 0 0 = BCD 8?
[1]

Add 6 correction 0 1 1 0 Correction necessary

1 0 0 0 0 1 1 0 = BCD 86

Q2 (a) Briefly describe the function of EACH of the following types of register found in the CPU of a typical microprocessor

- (i) instruction
- (ii) program counter
- (iii) memory address
- (iv) accumulator
- (v) status
- (vi) stack pointer
- (vii) index.

(b) Explain what is meant by a 'shift register' and give two examples of its use in a microprocessor.

A2 (a) [Tutorial Note: Sizes of registers described in the following answers refer to typical 8 bit microprocessors.]

(i) The instruction register is used to hold an instruction while it is being decoded to determine the actions necessary to execute the instruction.

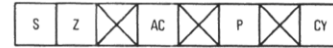
(ii) The microprocessor executes a program stored within its memory by reading each instruction sequentially. The program counter is used to keep a record of the address within the memory unit of the location which holds the next instruction to be executed. Since the program counter holds a memory address, it is comprised of 16 bits.

(iii) Several microprocessor instructions specify the address of a memory location within them for use as an operand. A 16 bit register (or pair of 8 bit registers), known as the *memory address register*, is used to hold this operand address during the execution of the instruction.

(iv) The accumulator (commonly called the *A register*) is used to hold one of the values to be operated on by the arithmetic logic unit during an appropriate arithmetic or logical instruction. The result produced by the instruction is normally placed in the accumulator and hence replaces or overwrites its existing contents.

(v) To enable binary data stored within a microcomputer to be interpreted by the user in different ways, microprocessors are provided with a set of flags (commonly called the *status register*). A typical example of a status register is shown in the sketch.

[Tutorial Note: Students would not be expected to define or explain the contents of a status register.]



S: Sign flag Z: Zero flag AC: Auxiliary carry flag P: Parity flag CY: Carry flag

(vi) The stack is normally implemented in a microcomputer system as part of the normal memory space. It is used as a last-in first-out buffer for subroutine handling. The stack pointer is a 16 bit register which holds the address in memory of the top of the stack; this readily enables the entry or removal of values.

(vii) The index register is a 16 bit register used to provide an operand address which is modified by adding an address value specified within an instruction. The resultant address provides the actual operand address. The indexed mode of addressing is very convenient when operands arranged in tables are accessed. Although some microprocessors may not have an index register as such, a form of indexed mode addressing can be used because arithmetic operations can be performed on register pairs used for memory addressing.

(b) A shift register is used to store a serial string of binary digits which on the application of a clock pulse can be displaced (for example, a displacement to the left in effect multiplies the contents by 2).

The arithmetic logic unit contains a shift register which would be used by the rotate instructions. A shift register can also be found in the peripheral interface and enables serial data to be converted to parallel.

Q3 (a) Explain what is meant by the following types of program language and state an application of where EACH may be used:

- (i) assembler
- (ii) high level.

(b) Assuming that the initial contents of register A are unknown, draw the flowchart of a program which will add 30_H to the contents of register A provided that the current contents of register A are zero. If register A contains a non-zero value, then 40_H must be added.

(c) From the flowchart in (b), write a program in one of the given machine codes in Table 1 or Table 2 attached. You should set out your answer using the headings and format shown in Fig. 1 below

PROGRAM TITLE:

ADDRESS	DATA OR INSTRUCTION	LABEL	MNEMONIC	COMMENT

Fig. 1

A3 (a) (i) An assembler program language consists of instructions represented in symbolic notation form. For example a machine instruction would be represented as:

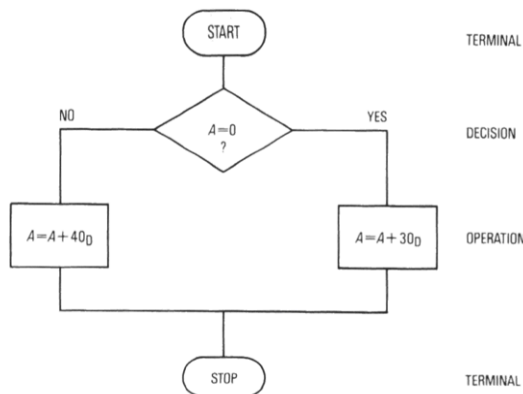
Operation mnemonic ▽ Symbolic address (▽ = space)

The operation mnemonic represents the operation code part of the instruction and hence the order to be performed. The symbolic address is the operand or address part. An assembler instruction can occupy one, two or even three bytes of memory and as such provides a very explicit and efficient means of programming. For this reason, assembler program language is commonly used for the handling of input/output devices which are very register conscious.

(ii) A high-level language consists of statements very often close to spoken language. Each statement is implemented by several machine instructions. For this reason, high-level languages tend to be inefficient in terms of machine time or storage. High-level languages have the advantage of being suitable for use by non-specialist programmers; for example, sales, accounting and management personnel. BASIC is one of the most common high-level languages used for general programming applications such as accounting, text handling, etc.

[Tutorial Note: The decision element of the flowchart shown in the sketch tests the contents of register A and sets appropriate condition flags. The condition flags enable the relevant operation to be selected.]

(b)



(c) [Omitted, machine dependent.]

Q4 With reference to the microprocessor instruction sets attached

(a) explain what is meant by EACH of the following

- (i) symbolic notation
- (ii) operation mnemonic
- (iii) symbolic address.

(b) Describe, using simple assembler code programming examples, the use of EACH of the following jump/branch instructions

- (i) unconditional jump
- (ii) jump/branch if plus
- (iii) jump/branch if not zero
- (iv) jump/branch if carry is set
- (v) jump/branch if parity even.

A4 (a) [Content overlaps substantially with Q3.]

(b) [Omitted, machine dependent.]

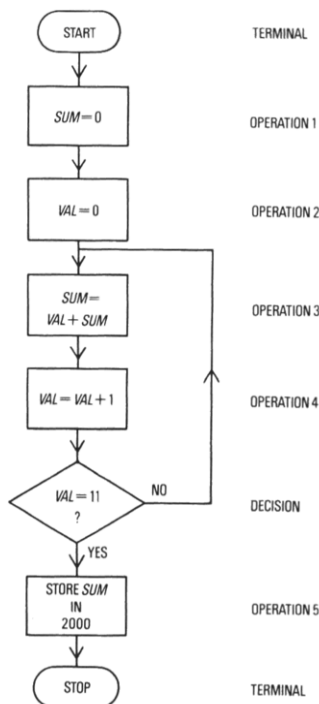
Q5 (a) Explain what is meant by a program loop.

(b) Draw the flowchart of a program using a loop which will add together the numbers 1_D to 10_D and store the result in memory location 2000_H .

(c) From the flowchart in (b) write a program in ONE of the given assembler codes in Table 1 or Table 2 attached. You should set out your answer using the headings and format shown in Fig. 1.

A5 (a) A program loop is a series of instructions in a computer program which may be repeated until an end condition is satisfied.

(b)



[Tutorial Note: Symbols SUM and VAL would be represented by internal microprocessor registers.]

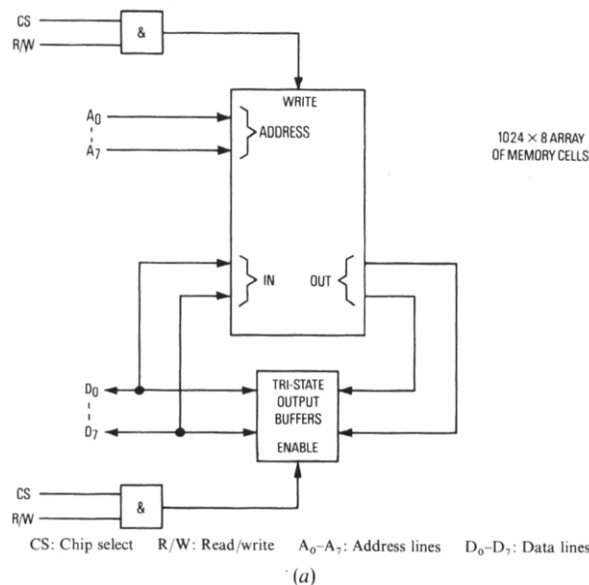
(c) [Omitted, machine dependent.]

Q6 (a) Draw a block schematic diagram to show all the bus and control connections of a typical 1024×8 bit RAM integrated circuit (IC).

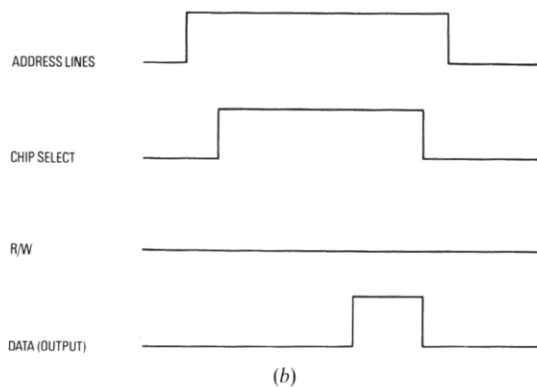
(b) With the aid of timing diagrams explain the operation of the RAM in (a) during

- (i) a read cycle
- (ii) a write cycle.

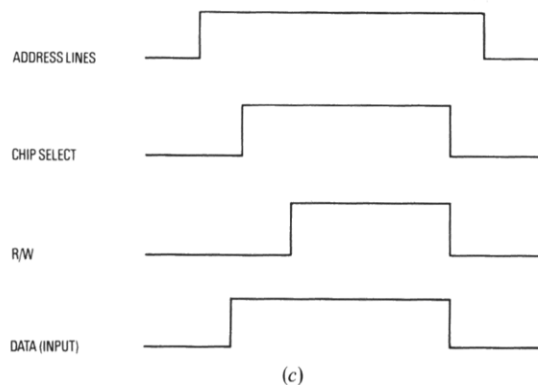
A6 (a) See sketch (a).



(b) (i) Sketch (b) shows the timing diagram during a read cycle of the random-access memory (RAM).


To read data from the RAM, the address of the appropriate location is presented on the address lines and the CHIP SELECT (CS) input is then activated. If the READ/WRITE (R/W) line is inactive ($R/W = 0$), then data is made available on the data lines via the tri-state output buffers.

(ii) Sketch (c) shows the timing diagram during a write cycle of the RAM.



To write data, the address of the appropriate location is presented on the address lines and the CS input is then activated. If the R/W line is active (R/W at logic 1), then the current value on the data lines is gated via the tri-state buffers and written to the addressed location.

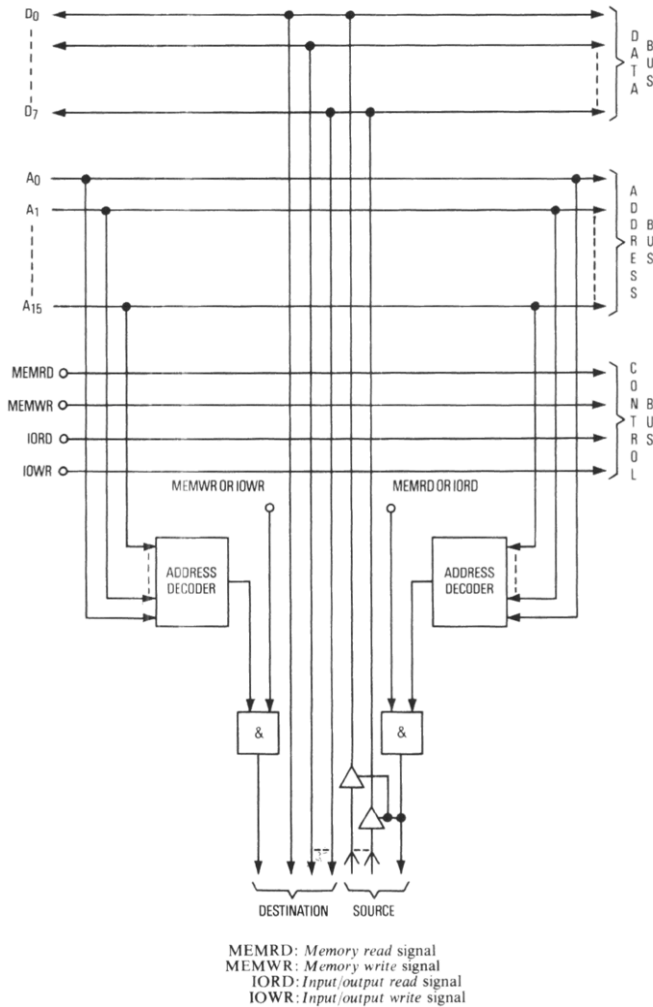
Q7 (a) Explain why address decoding logic is necessary in the bus structure of a typical microprocessor.

(b) Draw a block schematic diagram illustrating the bus structure of a typical microprocessor system which includes address decoding.

(c) With the aid of a truth table, explain the operation of a two-input address decoder and show how it can be implemented using two-input AND gates and inverters.

A7 (a) Address decoding logic is necessary in the bus structure of a microprocessor to enable the selection of specific memory addresses, either random-access memory (RAM) or read-only memory (ROM). Address decoding logic is also used to select input/output (I/O) device ports involved in a bus transfer request.

(b) See sketch (a).

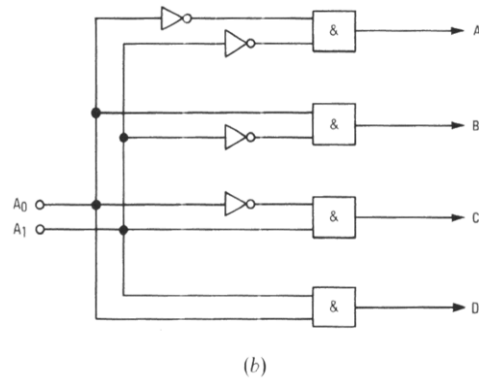


(c) The truth table for a two-input address decoder is shown below.

A ₁	A ₀	Device
0	0	A
0	1	B
1	0	C
1	1	D

From the truth table, it can be seen that device A is selected when both address lines A₀ and A₁ are both logic 0 (the other outputs are logic 0). Similarly, device B is selected when A₀ is logic 1 and A₁ logic 0 (the other outputs are logic 0), and so on.

A two-input address decoder can be implemented by using two-input AND gates and inverters as shown in sketch (b).

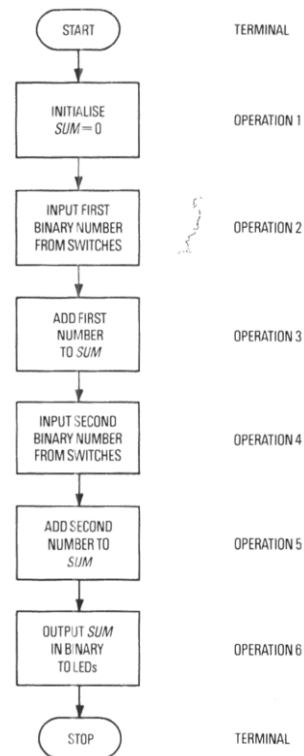


Q8 A set of eight switches are connected to an input port and eight light-emitting diodes (LEDs) are connected to an output port. Assume both ports are initialised.

(a) Draw a flowchart of a program which will input two binary numbers from the switches, add them together and output the result to the LED display in binary.

(b) From the flowchart in (a) write a program in ONE of the given assembler codes in Table 1 or Table 2 attached. You should set out your answer using the headings and format shown in Fig. 1.

A8 (a)



(b) [Omitted, machine dependent.]

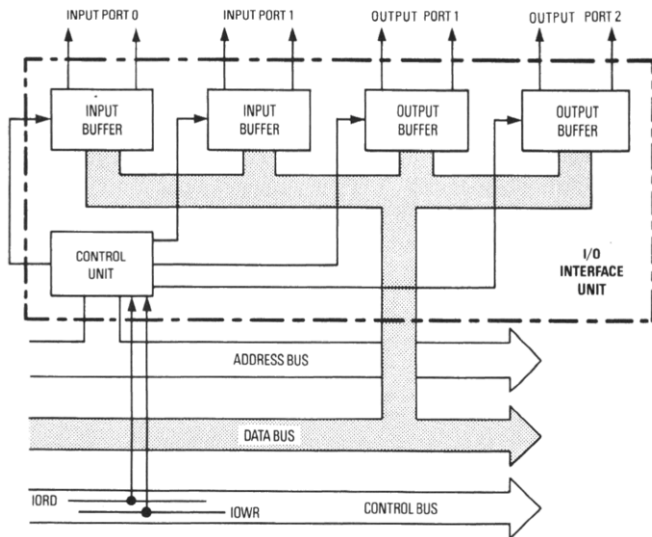
Q9 (a) Describe with the aid of a block diagram the read/write operation of a typical microprocessor four-port I/O interface unit showing the relevant connections to the address, data and control bus.

(b) Draw a timing diagram representing two consecutive instructions to input and to output data to the interface unit in (a). Indicate on the diagram fetch and execute cycles for EACH instruction.

A9 (a) Sketch (a) shows a block diagram of a typical microprocessor four-port input/output (I/O) interface unit.

Read Operation

To read a value from an input port, the microprocessor places the address of the appropriate port on the address bus and generates an input/output read (IORD) signal. The I/O interface unit then responds by placing the contents of the addressed port input buffer onto the data bus and this in turn is loaded into the accumulator.

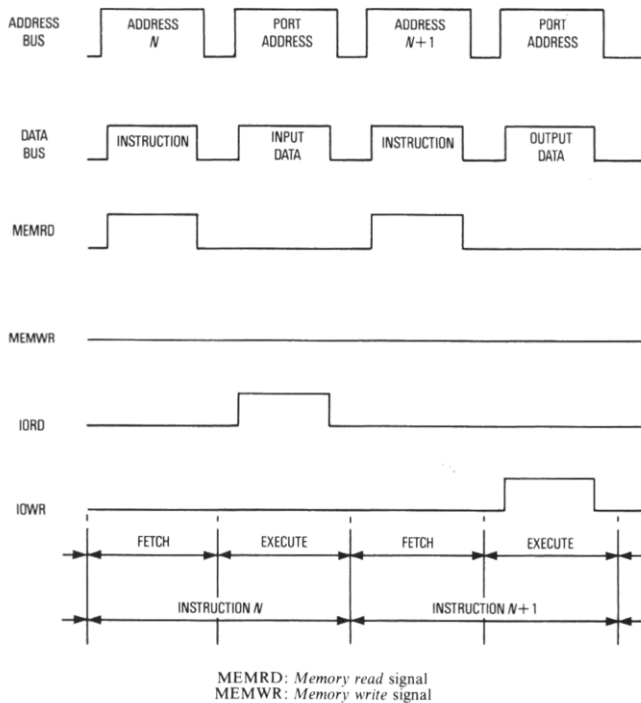


(a)

Write Operation

To write a value to an output port, the microprocessor places the port address on the address bus, places the data to be output on the data bus and generates an input/output write (IOWR) signal. The I/O interface unit then responds by placing the value on the data bus into the output buffer associated with the addressed output port to await being taken by the output device.

(b) See sketch (b).



(b)

Q10 (a) Explain, with the aid of an example, why EACH of the following interface characteristics may be necessary in a typical microprocessor/peripheral connection

- code conversion
- bus expansion

- timing control
- electrical buffering.

(b) With the aid of a truth table, explain how a tri-state device may be used as a buffer.

A10 (a) (i) Code conversion provides conversion between different types of binary code. A typical example is the conversion of hexadecimal to ASCII code for printers.

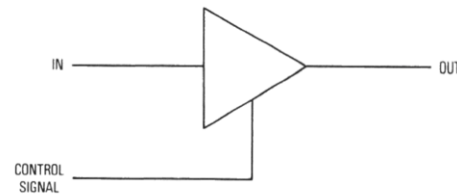
[Tutorial Note: ASCII, standing for American Standard Code for Information Interchange, is a 7 bit code representing the alphabet, numbers 0-9 and standard symbols.]

(ii) Bus expansion allows many lines to be converted to a few lines, or vice versa; this process is commonly known as *multiplexing/demultiplexing*. An example is the connection of several peripherals to the data bus.

(iii) Timing control enables data to be transmitted at different speeds (baud rates), which is necessary for parallel-to-serial conversion and vice versa. A typical example is the connection of a visual display unit (VDU), which is a serial device.

(iv) Electrical buffering converts voltages to different levels as required. An example is the conversion from transistor-transistor logic (TTL) levels of 0-5 V to the RS232 levels of -12 to +12 V for serial transmission.

(b) See sketch (a).

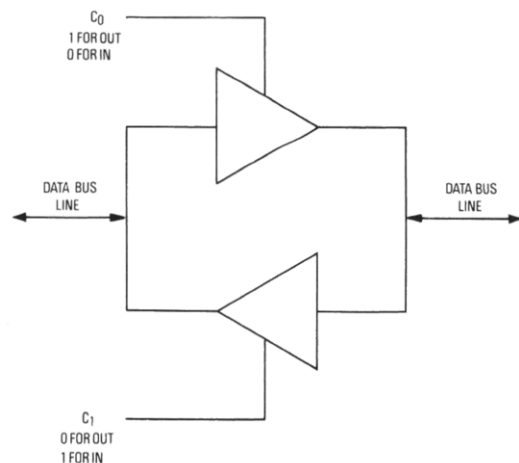


In	Control	Out
1	1	1
0	1	0
1	0	OFF
0	0	OFF

(a)

From the truth table, it can be seen that, when the control signal is logic 1, the device operates as if the IN and OUT terminals are connected together (short circuit). When the control signal is logic 0, the OUT terminal is effectively disconnected from the IN terminal (open circuit). A single tri-state gate can therefore be used as a unidirectional buffer.

A bidirectional buffer is constructed from two tri-state gates as shown in sketch (b).



(b)

Answers contributed by G. Illingworth

BUSINESS AND TECHNICIAN EDUCATION COUNCIL

National Certificate in Telecommunications

Sets of model questions and answers for Business and Technician Education Council (BTEC) units are given below. The questions illustrate the types of questions that students may encounter, and are useful as practice material for the skills learned during the course.

Where additional text is given for educational purposes, it is shown within square brackets to distinguish it from information expected of students under examination conditions. Representative time limits for questions are shown, and care has been taken to give model answers that reflect these limits.

We would like to emphasise that the questions are not representative of questions set by any particular college.

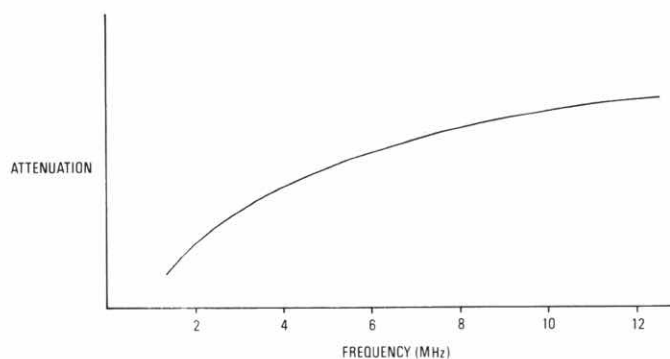
BTEC: TRANSMISSION SYSTEMS III

The questions in this paper are based on BTEC's standard unit U81/741. Students are advised to read the notes above

Q1 (a) Draw and label a graph of the attenuation/frequency response of a coaxial cable. Show typical frequency values on the x-axis.

(b) State the effect of increasing the diameter of the inside of the outer conductor. (4 min)

A1 (a)



(b) The attenuation (loss) is reduced.

Q2 The following are the diameters of the conductors of three audio cables.

- (a) 0.63 mm
- (b) 0.9 mm
- (c) 1.27 mm

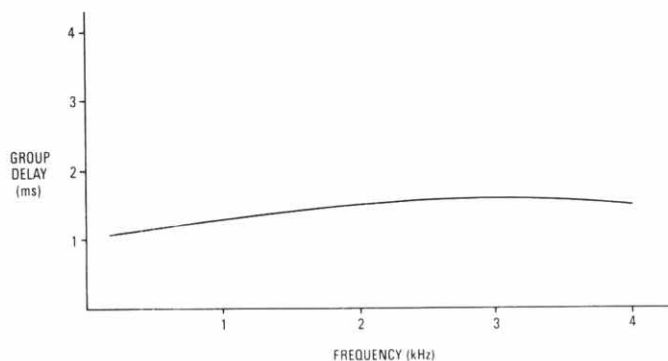
State which cable has the minimum attenuation per kilometre over an operating frequency range of 0–4 kHz. (1 min)

A2 (c) 1.27 mm

[Tutorial Note: In general terms, the lower the frequency, the less is the loss per kilometre. Also, the larger the conductor size, the less is the loss per kilometre.]

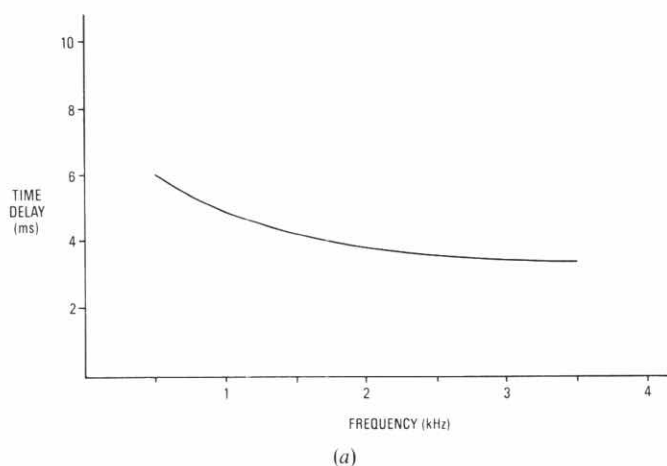
Q3 Draw and label a graph of the group delay/frequency curve of an unloaded audio cable. (4 min)

A3

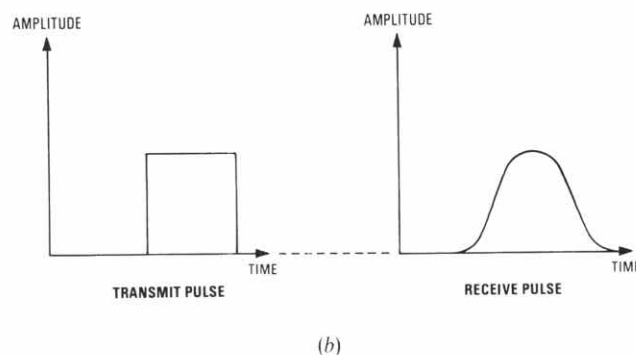


Q4 Explain with the aid of diagrams the term 'group delay' and how it affects data transmissions. (10 min)

A4 A signal transmitted in any medium takes a finite time to reach its destination. In a cable, the higher the frequency of a signal, the shorter the time it takes. (See sketch (a).) The time delay given in sketch (a) is the duration of time for signals at different frequencies to reach their destination over the same length of cable. As the cable length increases, so does the time delay; it is the difference in time-delay times over a group of frequencies that is important, and not the actual duration of propagation. This is called group delay, and is measured in units of time.



A few milliseconds of delay is of no consequence to the human ear, but the effect on data transmission can be serious especially with high-speed circuits. Signals that convey data consist of pulses made up of numerous frequencies, and, as described above, different frequencies have different delay times. It is possible that the frequencies making up the bulk of the pulse shape get significantly out of step with each other to an extent where the pulse is no longer recognisable as a pulse when it is received. (See sketch (b).)



Q5 Explain briefly the term 'skin effect' on a conductor. (5 min)

A5 The effective resistance of a conductor carrying alternating current increases with frequency as a result of the skin effect. As the frequency increases, the currents tend to flow near the surface of the conductor only, and this produces an apparent increase in resistance of the conductor; that is,

$$\text{AC resistance} = K\sqrt{f} \text{ ohm/unit length,}$$

where K is a constant derived from the primary coefficients and f is the frequency. For a given high frequency, the greater the conductor diameter, the less is the loss due to the skin effect.

Q6 Briefly explain why double-current working allows for faster signalling than single-current working. (4 min)

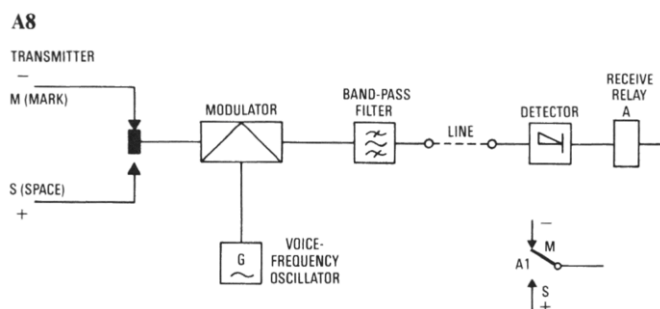
A6 Reversal of polarity in double-current systems assists the discharge of line capacitance, and this increases the initial rate of growth and decay currents, and makes it possible to achieve higher signalling speeds.

Q7 Explain the difference between simplex and duplex working. (4 min)

A7 Simplex is a method of working between two communications devices in which the transmission of information can take place in one direction only at a time.

Duplex is a method of working between two communications devices in which the transmission of information can take place simultaneously in both directions over a common path.

Q8 Sketch a basic block diagram for a voice-frequency signalling system. (4 min)

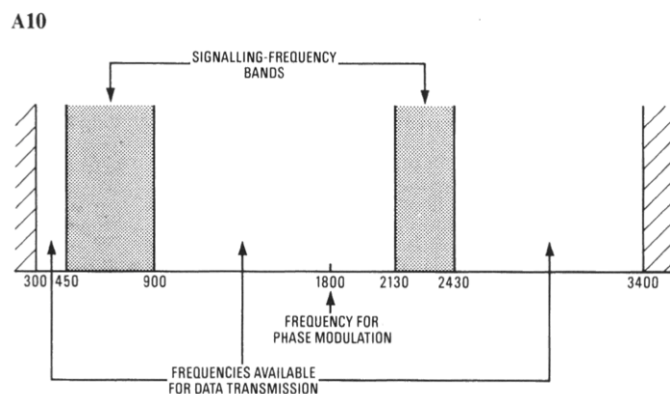


[Tutorial Note: The filter reduces the number of frequencies at the output of the modulator so that only two side frequencies caused by the transmitted DC signal are sent to line. At the receiver, voice-frequency currents, which constitute MARK signals, are rectified to produce DC signals that actuate the relay.]

Q9 Briefly explain the term 'frequency shift keying' (FSK). (4 min)

A9 In practice, frequency modulation of a data signal is achieved by using two different frequencies to represent the two binary digits 1 and 0. The process used is to shift the modulated signal from one frequency to the other for a corresponding change in amplitude of the data signal.

Q10 Sketch a diagram to show the bandwidth available for data transmission over the public switched telephone network. Indicate the signalling frequency bands and a common frequency for phase-modulation transmission. (4 min)

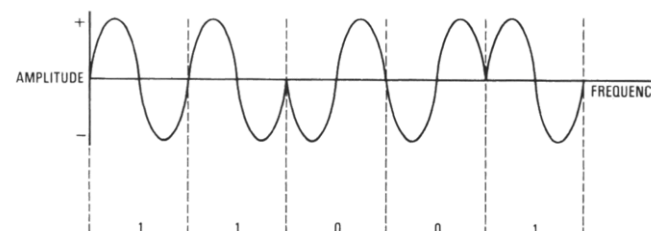


Q11 Determine the digital signal information present in the phase-modulated waveform shown in Fig. 1. Each cycle of the waveform represents one binary digit, the first digit being binary 1. (2 min)



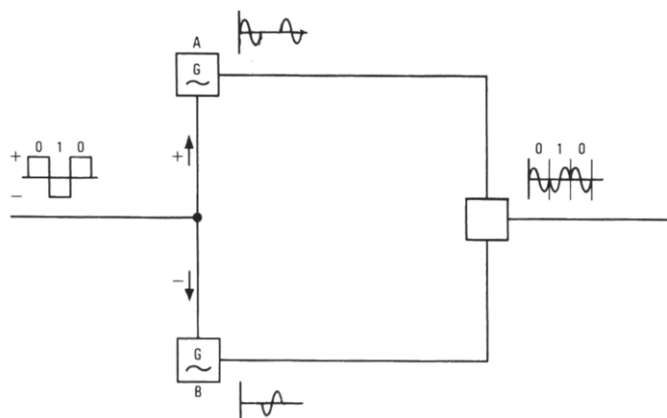
Fig. 1

A11



Q12 Draw and briefly explain a block diagram of a device for changing data into a phase-modulated analogue signal. Indicate on the diagram waveshapes at significant points. (10 min)

A12 The sketch shows two generators, A and B, both of the same frequency but 180° out of phase. When a binary 0 is received at the input, it is detected by generator A, which sends its frequency. When the input changes to a binary 1, generator A stops sending and generator B then starts sending, but the output of this generator is 180° out of phase. When another binary 0 is received, generator A is started again and so on. The outputs of the generators are then combined together so that the output is a continuous frequency with changing phase. This type of modulation is called phase-inversion modulation.



Q13 In phase modulation, the modulation rate, bit rate and number of phase states are related.

(a) State this relationship.

(b) Calculate the modulation rate of a data signal that has a speed of 9600 bit/s and four phase states. (6 min)

A13 (a) The relationship is

$$R = M \log_2 n \text{ baud,}$$

where R is the bit rate or data speed,
 M is the modulation rate, and
 n is the number of phase states.

(b) $R = M \log_2 n \text{ baud.}$

$$\therefore M = \frac{R}{\log_2 n} \text{ baud.}$$

$$\begin{aligned} \therefore M &= \frac{9600}{\log_2 4}, \\ &= \frac{9600}{2}, \\ &= 4800 \text{ baud.} \end{aligned}$$

[Tutorial Note:

$$\log_2 4 = \frac{\log_{10} 4}{\log_{10} 2} = \frac{0.6020}{0.3010} = 2.]$$

Q14 Calculate the bandwidth required for a circuit having a data speed of 600 bit/s and two carrier frequencies of 1000 Hz and 1600 Hz. (4 min)

A14 The bandwidth, B , is given by

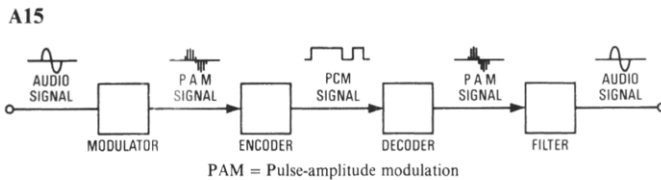
$$B = 2R + f_2 - f_1,$$

where R is the bit rate or data speed,
 f_1 is the lower carrier frequency, and
 f_2 is the higher carrier frequency.

Substituting the given values gives

$$\begin{aligned} B &= (2 \times 600) + 1600 - 1000, \\ &= 1200 + 1600 - 1000, \\ &= 1200 + 600, \\ &= 1800 \text{ Hz.} \end{aligned}$$

Q15 Draw and label a block diagram of a pulse-code modulation (PCM) system for one direction of transmission only. Include on the diagram blocks of waveforms where there is a change of signal shape. (4 min)



Q16 In a pulse-code modulation system, what quantum levels do each of the following binary codes represent?

- (a) 00001001
- (b) 00011100
- (c) 10000011
- (d) 10000110

(4 min)

- A16** (a) -9
 (b) -28
 (c) +3
 (d) +6

[Tutorial Note: Seven binary digits are required to represent numbers from 0-127. An additional 1 or 0 placed before the binary seven digits indicates a positive or negative number, respectively. Therefore, eight binary digits give 256 quantum levels.]

Q17 Calculate the bit rate of a 20-channel pulse-code modulation system that uses an 8 bit word, and each channel has a peak frequency of 5 kHz. (3 min)

$$\begin{aligned} \text{A17 Bit rate} &= \text{sampling frequency} \times \text{number of binary bits per word} \\ &\quad \times \text{number of channels in the system,} \\ &= (5 \times 2) \times 8 \times 20 \text{ kbit/s,} \\ &= 1.6 \text{ Mbit/s.} \end{aligned}$$

[Tutorial Note: Satisfactory reconstruction of an original signal transmitted by using pulse-code modulation can take place provided that the sampling frequency is at least equal to or greater than twice the highest frequency in the signal being transmitted.]

Q18 (a) State the three factors on which the bandwidth required for a pulse-code modulation (PCM) system is dependent.

(b) Calculate the bandwidth for a PCM system that has a bit rate of 1.536 Mbit/s and a frequency range from DC up to the fifth harmonic of the highest fundamental frequency. (5 min)

A18 (a) The bandwidth of a PCM system is dependent upon:

- (i) the method of transmitting binary digits,
 - (ii) the transmission rate, and
 - (iii) the range of frequencies required for successful detection.
- (b) The highest fundamental frequency, f_1 , is given by

$$f_1 = \text{bit rate}/2.$$

$$\therefore f_1 = \frac{1.536}{2} = 768 \text{ kHz.}$$

The fifth harmonic

$$= 5 \times 768 \text{ kHz} = 3.84 \text{ MHz.}$$

Therefore, the bandwidth is 3.84 MHz.

Q19 Explain why there is a need for the regeneration of pulse-code modulation signals. (8 min)

A19 Digital signals are attenuated and distorted in the process of transmission, as are analogue signals, but, because of their different nature, different means of correction are possible. For analogue signals amplifiers are used to overcome attenuation and equalizers to correct distortion. For a binary digital signal, all that is required is a pulse to be present or absent at a particular instant in time; the shape of the pulse is unimportant as far as the information it contains is concerned. A badly attenuated or distorted pulse could look like noise and corrective action must take place before this occurs. This consists of replacing the distorted pulse with new ones having the same properties as the original pulses before transmission. This process, known as *regeneration*, is performed by a regenerator. The incoming signal is inspected at each time interval for the presence or not of a pulse, and either a new correctly shaped pulse is transmitted or no pulse at all. Noise and distortion are not passed on from regenerator sections and the overall performance of the link is virtually independent of link length.

Q20 Give three reasons for synchronisation of digital line systems. (3 min)

A20 Synchronisation is necessary

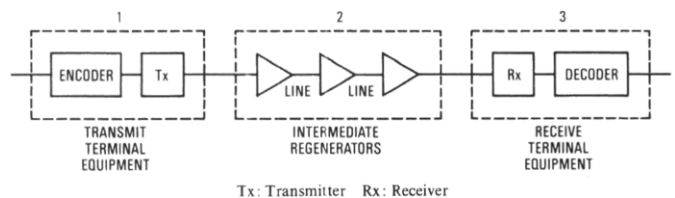
- (a) to minimise speech distortion,
- (b) to eliminate data signal errors, and
- (c) to ensure that customers are correctly connected to each other.

Q21 State two types of semiconductor light sources and the materials from which they are made. (3 min)

A21 Two types of semiconductor light sources are light-emitting diodes (LEDs) and lasers. Both devices are made from the semiconductor materials gallium arsenide and gallium aluminium arsenide.

Q22 Sketch the three fundamental parts of an optical-fibre transmission system. (4 min)

A22 The three fundamental parts are indicated by blocks 1, 2 and 3 in the sketch.



Q23 State four advantages of optical fibres over metallic cables. (4 min)

A23 Any four of the following advantages:

- (a) The bandwidth can be very large therefore it has a high transmission capacity.
- (b) The potential cost of producing fibres is low.
- (c) The physical cable size is small.
- (d) Crosstalk between fibres is negligible.
- (e) It has a high immunity to outside interference.
- (f) It has complete electrical isolation.
- (g) The spacing of intermediate regenerators is large compared with the spacings used on metallic cables.

[Tutorial Note: These advantages show that optical fibres are a better prospect for future communications than metallic cables.]

Questions and answers contributed by P. Ritchie

BTEC: TELEPHONE SWITCHING SYSTEMS II

The following questions are based on the BTEC's standard unit U81/753. Students are advised to read the notes on p. 56

Q1 Explain what is meant by 'traffic intensity' in telecommunications. (2 min)

A1 In telecommunications, traffic intensity refers to the average number of simultaneous calls in progress.

Q2 For a Strowger-type telephone exchange, state a typical grade of service between the penultimate and final selector stage. (2 min)

A2 0.02 or 1/50 or one call lost in 50.

Q3 A 200-outlet group selector stage has the following trunks to the next stage:

- Level 1 ... 5
- Level 2 ... 51
- Level 3 ... 43
- Level 4 ... 18
- Level 5 ... Nil
- Level 6 ... Nil
- Level 7 ... 15
- Level 8 ... 21
- Level 9 ... 30
- Level 0 ... 26

- (a) Which levels have full availability?
- (b) Which levels require a grading scheme?
- (c) Which levels, when dialled, may result in the following signals being returned to the caller?

- (i) number-unobtainable (NU) tone,
- (ii) equipment-engaged tone, and
- (iii) busy tone.

(5 min)

A3 (a) Levels 1, 4 and 7.

(b) Levels 2, 3, 8, 9 and 0

(c) (i) NU tone is returned to the caller if level 5 or 6 is dialled.

(ii) Equipment-engaged tone is returned to the caller if all the working outlets of a level are already in use. This applies to levels 1, 2, 3, 4, 7, 8, 9 and 0.

(iii) A group selector stage does not originate busy tone. This tone originates from the final selector stage.

Q4 During a one-hour period, 2448 calls were observed passing through a switching stage. If the average duration of a call was 2.4 min, determine the traffic intensity of the stage. (3 min)

A4 Let A = the traffic intensity,
 C = the total number of calls,
 t = the average duration of a call in minutes, and
 T = the observation period in minutes.

Then,

$$A = \frac{Ct}{T} = \frac{2448 \times 2.4}{60} = 97.92 \text{ erlangs.}$$

Q5 Why do charts showing traffic flow through a Telex exchange over a 24-hour period differ from those of traffic flow through a telephone exchange. (10 min)

A5 Generally, on a telephone call, information flows from caller to called party and from called party to caller for the duration of the call. Also, in most cases, a call cannot be established unless the called party is available to answer the call. Thus the flow of traffic in a telephone exchange is concentrated during the working period of the day and, to a lesser extent, to the period just after 18.00 hours when customers take advantage of the cheap rate. The Telex system is not dependent on the presence of an operator at the called end of a Telex line as Telex terminal stations are capable of identifying the called line, and of receiving the caller's instructions automatically. Thus, the Telex system does not need to operate within the working period of the day only. Also, compared with telephone calls, a greater proportion of most Telex calls is received from, and transmitted to, overseas terminals. Telex traffic is therefore spread over the full 24-hour period, and traffic charts are based on incoming calls, or outgoing calls only.

Q6 Explain the term 'grade of service'. (3 min)

A6 Grade of service refers to the proportion of calls that are allowed to fail in the busy hour owing to the limitation, for economic reasons, of the amount of switching plant.

The grade of service can be expressed by the ratio

$$\text{grade of service} = \frac{\text{number of calls lost}}{\text{number of calls offered}} = \frac{\text{traffic lost}}{\text{traffic offered}}$$

Q7 Why is it desirable to use traffic recording equipment in a telephone exchange? (6 min)

A7 The provision of exchange equipment and junction plant is based on predicted traffic flows. The prediction is made several years prior to the installation of the equipment. It is therefore essential for planning engineers to know if the actual level of traffic flow is in line with the predicted level as, if this is not the case, customers may be provided with a poor grade of service (the actual flow is much higher than predicted) or capital investment may be giving a poor financial return (the actual flow is much lower than predicted and therefore the plant is lying idle for unacceptably long periods). Traffic recording equipment is therefore used to monitor the flows of traffic.

Q8 In Fig. 1, clearly identify the busy hour. (4 min)

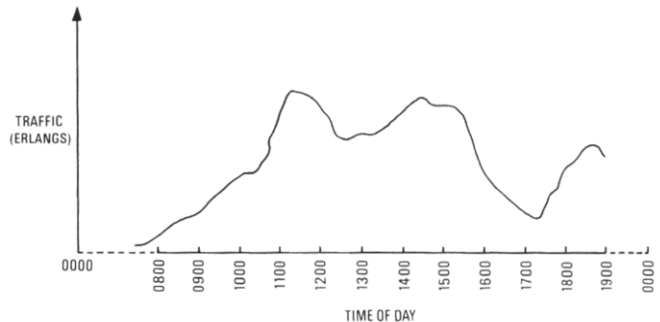
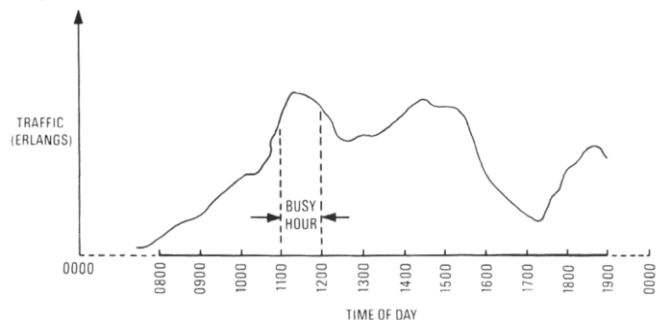


Fig. 1

A8 The busy hour of an exchange is determined from the hour-to-hour, or half-hour-to-half-hour intervals; no other reference points are used. The busy hour is therefore as shown in the sketch.



Q9 Identify the exclusive and shared equipment areas of the trunking diagram shown in Fig. 2. (4 min)

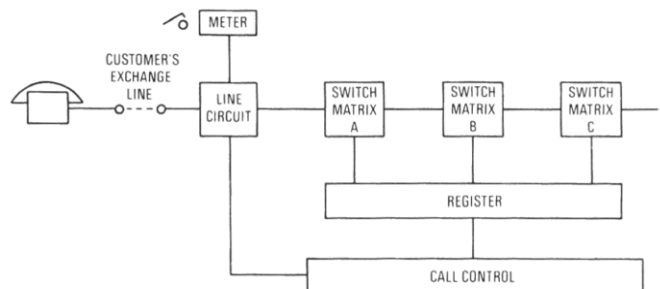
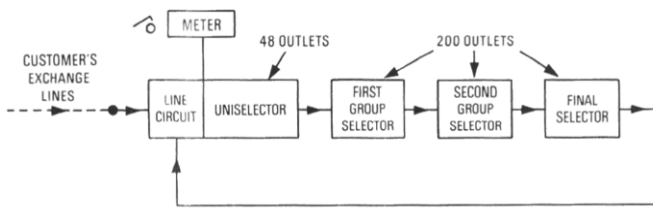


Fig. 2

A9 The customer's exchange line, line circuit, meter, the trunk between the line circuit and switch matrix A, and the trunk between the line circuit and the call control are all exclusive to the customer. The remainder of matrix switch A, switch matrices B and C and the register and call control are shared by a number of customers.

Q10 Draw a labelled block diagram of a Strowger-type 3000-line non-director telephone exchange. For each switching stage, indicate the maximum number of available outlets per switch. (10 min)

A10



Q11 List the tones that may be originated at the first group selector stage of a non-director Strowger-type telephone exchange and explain their purpose. (5 min)

A11 Dial tone, equipment-engaged tone, number-unobtainable tone.
Dial tone informs the caller that dialling may commence.
Equipment-engaged tone informs the caller that no equipment is available, at that time, for the continuation of the routing of the call.
Number-unobtainable tone informs the caller that a spare level or line circuit has been dialled.

Q12 What supervisory signals originate at the final selector stage of a Strowger-type director exchange? (5 min)

A12 Ring tone, ringing current, busy tone, number-unobtainable tone, metering pulses and called-customer-answer signal.

Q13 What is the function of the A-digit selector in a director telephone exchange? (5 min)

A13 The function of the A-digit selector is to return dial tone to the caller, to provide the caller with access to the director, to provide the caller access to the local register, and to provide the director and local register access to the first code selector.

Q14 State the name of the electronic unit which replaces the electromechanical director, local register and A-digit selector of a Strowger director exchange. (2 min)

A14 Stored-program control (SPC) unit.

Q15 For a local call in a director area, what digits do not need to be dialled by the customer? (2 min)

A15 The routing digits.

Q16 Hunters and finders are often used in Strowger systems; distinguish between the two. Include an explanatory diagram. (8 min)

A16 The essential difference between a hunter and finder circuit is the condition that exists at the input and output terminals of the circuit. A hunter has one input line and several output lines. A finder has many input lines and only one output line. (See sketch.)



In the line-circuit stage of a Strowger telephone exchange, hunters are provided to cater for high-calling-rate customers, and finders cater for low-calling-rate customers. Very often the two systems are combined to form a composite line-finder system.

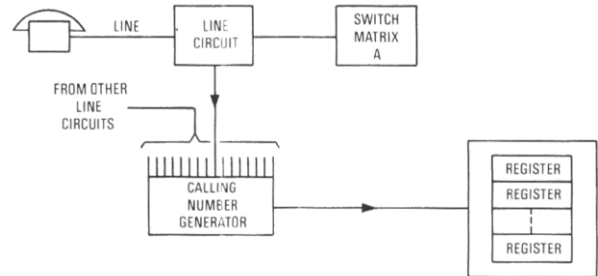
Q17 Two erlangs of traffic are offered to four trunks, which are arranged to provide a sequential search process. Determine the grade of service. (10 min)

A17 If the traffic offered to four trunks is A erlangs, then the grade of service

$$\begin{aligned} &= \frac{A^4}{4!} \\ &= \frac{A^4}{1 + A + \frac{A^2}{2!} + \frac{A^3}{3!} + \frac{A^4}{4!}} \\ &= \frac{2}{3} \\ &= \frac{2}{1 + 2 + 2 + \frac{4}{3} + \frac{2}{3}} \\ &= 0.047. \end{aligned}$$

Q18 Explain, with the aid of a block diagram, how a register in a TXE2 telephone exchange is initially accessed by a calling line condition. (10 min)

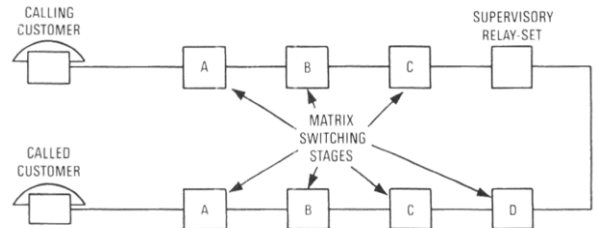
A18



See sketch. Each line circuit has an exclusive link to the calling number generator (CNG). When a call is initiated by a customer, the line circuit transmits a signal, via this link, to the CNG. As a result, the CNG accesses an available register and passes to this register the identity of the calling line in coded form. The CNG releases and the assigned register takes over the control of the call.

Q19 Draw a labelled trunking diagram of an established call in a TXE2 telephone exchange. (6 min)

A19

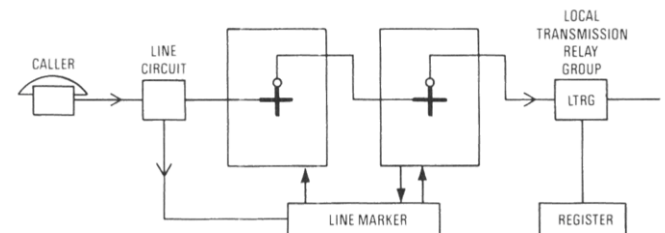


Q20 What is the function of the supervisory relay-set in a TXE2 telephone exchange? (5 min)

A20 The supervisory relay-set takes over the control of a call once the common control equipment has verified that a call path exists between the calling line circuit and the called line circuit. The relay-set provides ring tone, ringing current, metering and transmission-bridge facilities.

Q21 Explain, with the aid of a diagram, how a caller in a TXK1 telephone exchange is returned dial tone. (15 min)

A21



See sketch. The line circuit responds to a calling condition by signalling the line marker. The line marker instructs the distributor switch B (DSB), to which the calling line is connected, to access a free distributor switch A (DSA). The selected DSA switch is instructed by the line marker to select a free local transmission relay-group (LTRG) relay-set which must, however, have access to at least one free register. When the LTRG and register have been reserved, a signal is returned to the line marker. The line marker responds by instructing the DSB and DSA switches to operate the relevant crosspoints and the caller is extended through to the selected register. The line marker releases and the register returns dial tone to the caller.

Q22 How many line circuits can be connected to a distributor stage in a TXK1 exchange? (2 min)

A22 500 line circuits.

Q23 List the switching stages involved in an own-exchange call of a TXK1 system. (2 min)

A23 In sequential order:

distributor switch B (DSB),
distributor switch A (DSA),
router switch A (RSA),
router switch B (RSB),
DSA, and
DSB.

Q24 Where are TXK3 telephone exchanges normally used? (2 min)

A24 In director areas.

Q25 Explain the basic make-up of a line selection unit of a TXK3 system. (2 min)

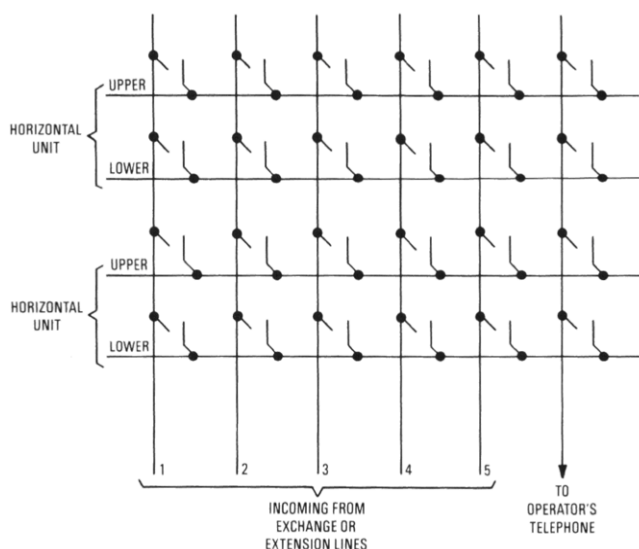
A25 The line selection unit comprises 500 line circuits, a marker unit and two crossbar switch stages.

Q26 In a TXK3 exchange, what unit controls the call after the call path has been established? (2 min)

A26 The local feed junctor.

Q27 Explain the basic principle of operation of the matrix used in small manual switchboard systems. (15 min)

A27



See sketch. Each crosspoint is controlled by a three-position switch. The switch has an upper, lower and central position. When the switch is in the central position, neither contacts of the crosspoint are operated, but, when in the upper or lower position, the associated contact is closed.

The switchboard matrix is operated by an operator, who is responsible for collecting the information from the caller and setting up the call path through to the called station. When a line circuit initiates a demand-for-

service signal, the operator selects a horizontal unit for the call. The calling line and the operator are then extended through to each other by the operation of either the upper or lower contacts. Consider, for example, that the upper contacts are used. Having ascertained the wanted line from the caller, the operator, using the same horizontal unit, operates the upper contact of the wanted line circuit. Ringing current is extended, by the operator, to the called line and, when the called party answers, the ringing signal is removed and the caller and called party are connected to each other via the operated crosspoints of the selected horizontal unit. The operator restores his/her own switch to the central position and is now able to handle further incoming calls by using another horizontal unit or the lower position of the horizontal unit already in use.

Q28 For the circuit shown in Fig. 3, determine the efficiency of the stage. (4 min)

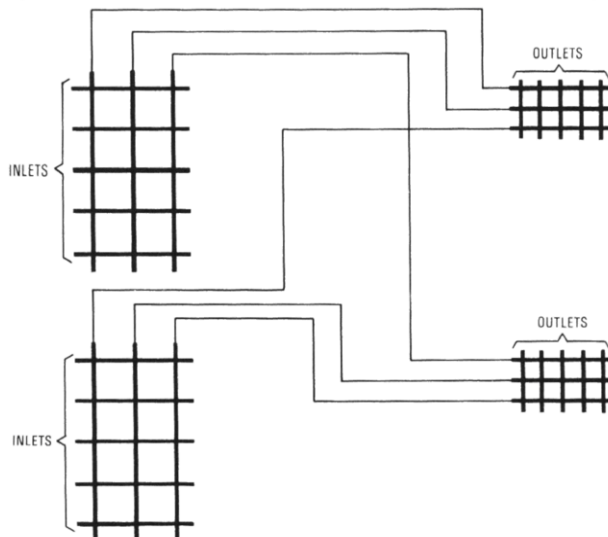


Fig. 3

A28 The efficiency of the switch matrix

$$= \frac{\text{maximum number possible simultaneous calls}}{\text{total number of crosspoints}} \%$$

$$= \frac{6}{60} \%$$

$$= 10\%$$

Q29 State the disadvantages of link trunking. (5 min)

A29 Two switching units are required as opposed to one.

Two crosspoints must be used to route the call through the switching stage.

The efficiency of the switching stage is reduced.

Calls may be blocked even though free outlets to the next stage are available.

Q30 State the methods used to minimise blocking in TXE2, TXK1 and TXK3 systems. (3 min)

A30 In TXE2 systems, a third switch is introduced to minimise blocking. In TXK1 and TXK3 systems, larger crossbar switches are used. Also, in TXK3 systems, a form of switch linkage, known as *interaid linkage*, is used to help minimise blocking.

Q31 Digits 389 are to be transmitted on a junction line. Compare the time taken by using

- a DC signalling system,
- a one-voice-frequency (VF) signalling system, and
- a multi-frequency (MF) signalling system.

(5 min)

A31 For systems (a) and (b), the speed of signalling would be that of a telephone dial; namely 10 pulses/s. Thus for these two systems, the time taken is the time required for each digit plus the inter-digit pause; that is,

$$\frac{3}{10} + \frac{3}{4} + \frac{8}{10} + \frac{3}{4} + \frac{9}{10} = 3.5 \text{ s.}$$

MF systems require about 160 ms per digit; thus the total time to transmit the three digits is $3 \times 160 = 480$ ms; no inter-digit pause is necessary.

Q32 Explain the basis of time-space-time switching as shown in Fig. 4. (10 min)

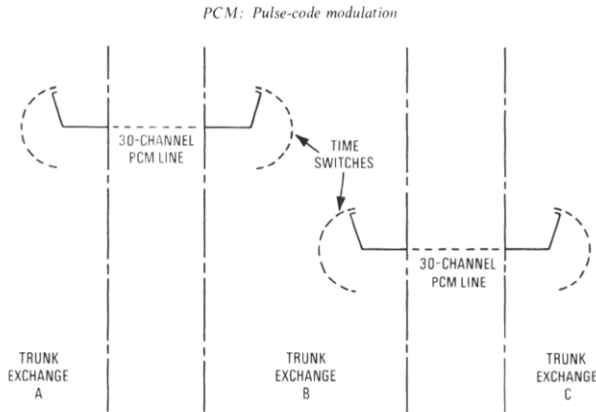


Fig. 4

A32 The 30-channel links between A and B, and between B and C employ time-division signalling. On a call between exchanges A and C, the time-slot allocated to the A-B link may not coincide with the time-slot allocated to the B-C link. Because all four time switches are synchronised, it is necessary to store the information arriving at B on the A-B link for a finite length of time. When the time-slot allocated to the B-C link is offered the B-C line, the stored information may then be transmitted. Switching information from a system with one time-base to another via a delay-storage unit is referred to as a *time-space-time system*.

Q33 Why is sidetone desirable in a telephone instrument? (5 min)

A33 A telephone is designed so that, whenever it is in use, a small level of sound from the transmitter of the same instrument is reproduced in the receiver. This is referred to as *sidetone*. If sidetone did not exist, the speaker would get the impression that the telephone was 'dead', and it would thus be very disconcerting to speak into.

Q34 Why is multi-frequency signalling employed on the transit network? (10 min)

A34 At the end of dialling a number, the caller would expect to hear ring tone or busy tone. If neither of these tones are heard fairly quickly, the caller invariably assumes that the call has been unsuccessfully routed through the system, and, as a result, hangs up. On long-distance calls routed through the transit network, the exchange code and the local number may need to be transmitted through more than one transit centre. As each transit centre involved with the routing of the call needs to receive and re-transmit these codes, an unacceptable post-dialling delay would result if the standard 10 pulses/s signalling speed was used. This is because the originating transit centre cannot commence signalling to the following transit centre until the caller has completed dialling. Signalling at 10 pulses/s would give a post-dialling delay typically in excess of 15 s, whereas multi-frequency signalling, which is a very-high-speed signalling system, would give a post-dialling delay of typically 2 or 3 s.

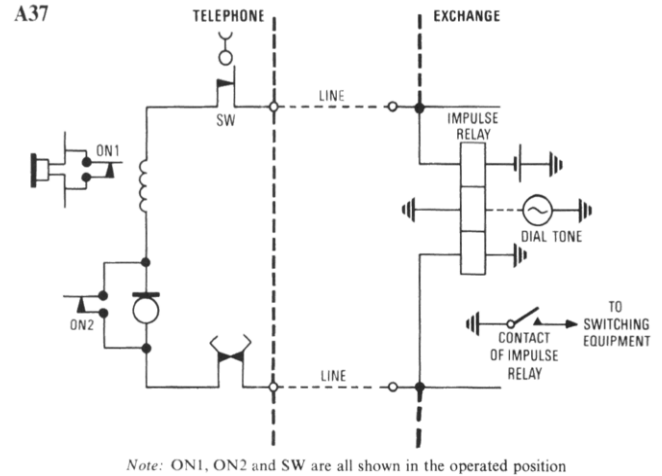
Q35 What two line parameters have a major influence on loop-disconnect signals? (2 min)

A35 Line resistance and line capacitance.

Q36 Explain the Telex term 'who are you'. (6 min)

A36 To complete a Telex call, there is no need for an operator to be present at the called terminal. However, it is essential that the caller be given a positive indication that the correct called party has been accessed. When the Telex exchange equipment has established a call path between the caller and called party, the Telex exchange transmits a *who are you* signal to the called line. This is a special code signal which automatically trips the answer-back mechanism at the called terminal and, as a result, the called Telex station transmits its identity down the send wire. This signal is received at the calling end and provides the caller with a positive identification of the distant terminal.

Q37 By using an elementary circuit diagram, explain how telephone dialling pulses are transmitted to, and absorbed by, the telephone-exchange equipment. (10 min)



See sketch. Dial tone is extended to the caller via a coil of the impulse relay at the telephone exchange. As soon as the dial is activated by the caller, the dial off-normal contacts short-circuit the telephone receiver and transmitter. During dialling, the dial pulse contacts periodically open and close the DC loop to the exchange. As a result, the impulse relay pulses, and one of its contacts signals the switching equipment. This switching equipment could be the two-motion selector mechanism in a Strowger-type exchange or the register in a common-control type exchange.

Q38 For each labelled junction in Fig. 5, state the signalling system used. (5 min)

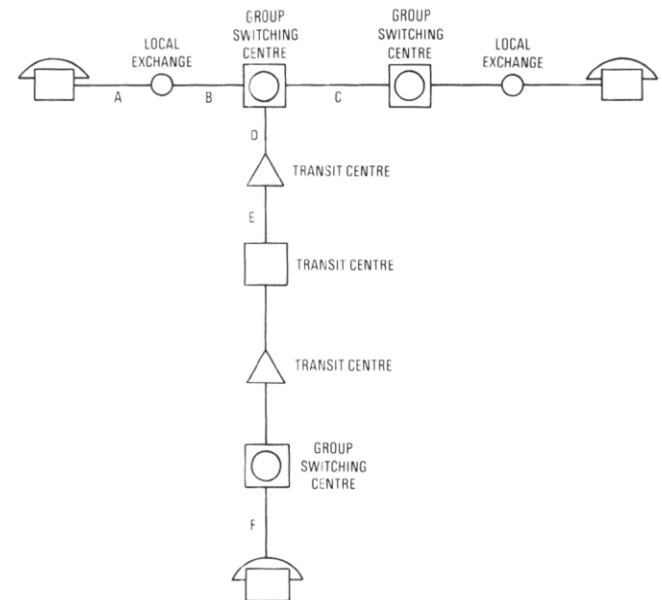


Fig. 5

- A38** (a) Loop-disconnect signalling.
- (b) Loop-disconnect signalling.
- (c) One-voice-frequency, DC2 or loop-disconnect signalling depending on the distance between the two centres.
- (d) Multi-frequency signalling.
- (e) Multi-frequency signalling.
- (f) Loop-disconnect signalling.

Q39 What is the function of the select finger of a crossbar switch? (3 min)

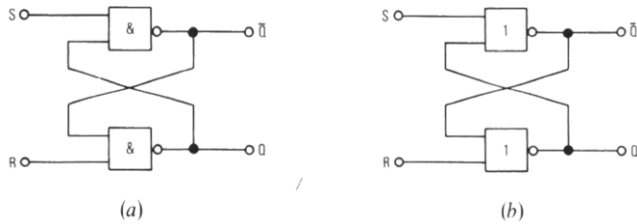
A39 The function is to hold the crosspoint contacts operated for as long as the associated vertical operating bar is operated. (The vertical operating bar is operated by the bridge magnet.)

Questions and answers contributed by N. C. Webber

The following questions are based on the BTEC's standard unit U81/751. Students are advised to read the notes on p. 56

Q1 An S-R bistable circuit can be constructed by using either two NAND gates or two NOR gates. Compare these two circuits by drawing their circuit diagrams and by deriving their truth tables. (7 min)

A1 The circuit constructed from NAND gates is shown in sketch (a), and that from NOR gates in sketch (b).



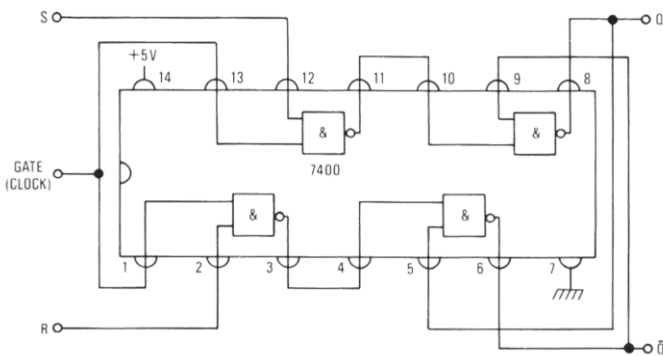
The truth tables are as follows

NAND Gates				NOR Gates			
S	R	Q	Q̄	S	R	Q	Q̄
0	0	1	1	0	0	Previous states	
0	1	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	1	Previous states		1	1	0	0

The circuits are similar in many respects apart from the output conditions during the 'indeterminate' state, with inputs S and R at logic 0 for the NAND circuit and inputs S and R at logic 1 for the NOR circuit. Here they assume opposite states. In addition, the circuits enter their 'memory' condition for different inputs; that is, with inputs S and R at logic 1 for the NAND circuit, and inputs S and R at logic 0 for the NOR circuit.

Q2 Show, with the aid of a diagram, how a 7400 logic circuit could be wired to construct a gated S-R bistable. (5 min)

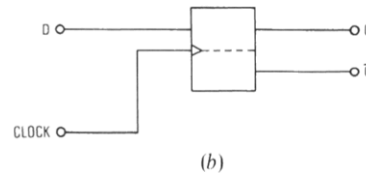
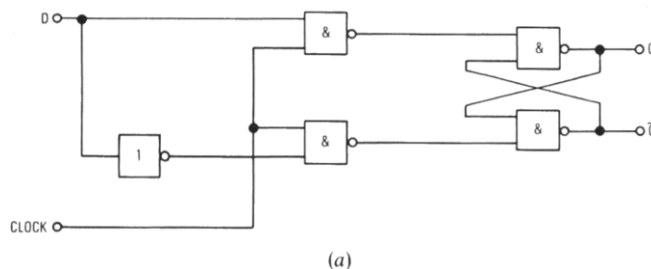
A2 The wiring of the 7400 quad two-input NAND gate is shown in the sketch. The internal gates are shown for clarity.



[Tutorial Note: Other pin connections could be used to achieve the same circuit and hence the same logical function.]

Q3 'A D-type bistable circuit is simply a modified gated S-R bistable.' Support this statement by drawing the circuit diagram of a simple D-type bistable circuit and then its normal circuit symbol. (5 min)

A3 The circuit in sketch (a) shows that, by adding a single inverter, a D-type bistable circuit can be constructed from a gated S-R bistable circuit. The normal circuit symbol is shown in sketch (b).



Q4 Explain the main problems associated with a gated S-R bistable circuit, and describe how they are overcome with a master-slave J-K bistable. (6 min)

A4 The two main problems associated with the S-R bistable circuit are (a) that it has an indeterminate state, when both outputs assume the same logic level; and

(b) that its output can change immediately in response to a change in the input while the clock pulse is in its logic 1 state. This is undesirable since synchronism with the clock is lost.

The J-K bistable is arranged to have no indeterminate state. If the two inputs to an S-R bistable are at logic 1, an indeterminate output results; but, if the J-K bistable circuit has similar inputs, its output simply changes state.

A master-slave J-K bistable changes its output state only on the negative-going edge of the clock pulse. No matter how many times the inputs change while the clock is at logic 1, only their condition when the clock goes to logic 0 is passed to the outputs.

Q5 The J-K bistable circuit shown in Fig. 1 works reliably only under certain conditions. Briefly explain what these conditions are and how this situation can be improved. (4 min)

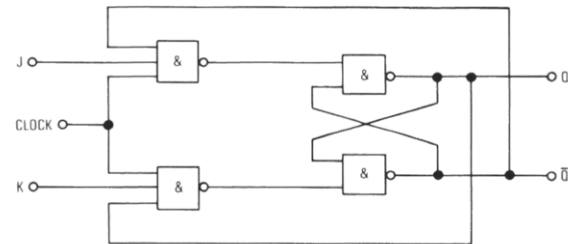


Fig. 1

A5 The circuit shown in Fig. 1 works reliably only when the duration of the clock pulse is less than the propagation delay of the circuit.

For example, if both inputs J and K are at logic 1, and the clock pulse rises to logic 1, the output changes state because of the cross-connections of outputs Q and Q-bar to the input gates. If the clock is still at logic 1, however, the outputs then change back to their original state, and the circuit oscillates for as long as the clock remains at logic 1.

The situation is best remedied by using a master-slave J-K bistable instead of the type shown in Fig. 1.

Q6 A master-slave J-K bistable circuit is shown in Fig. 2. Briefly explain the operation of the circuit when both inputs J and K are at logic 1 and a positive clock pulse occurs on the CLOCK input. Output Q is initially at logic 0 and Q-bar is at logic 1. (6 min)

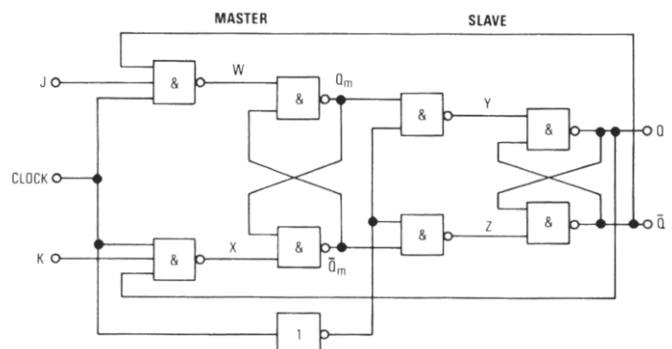


Fig. 2

A6 As the clock pulse rises from logic 0 to logic 1, the inverted clock pulse which drives the slave bistable changes to logic 0. This places the slave in its 'memory' condition, and prevents any output changes.

With the conditions indicated in the question, output Q-bar, input J and the

clock are all at logic 1; this produces logic 0 at point W in the circuit. Similarly, since output Q is at logic 0, point X becomes logic 1. These conditions cause point Q_m to become logic 1 and point Q_m to become logic 0.

When the clock pulse returns to logic 0 state, the master bistable is taken into its 'memory' condition in which no input changes can affect it. The slave clock, however, changes to logic 1, which causes the logic states at points Q_m and Q_m to be transferred to the Q and Q outputs of the slave circuit.

Q7 Name the type of bistable circuit which would generally be used for the following applications:

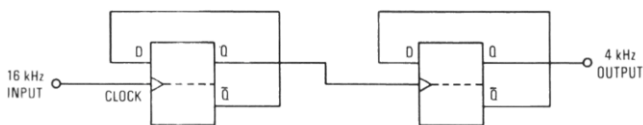
- a divide-by-3 synchronous counter,
- an 8 bit latch, and
- a switch debouncing circuit.

(3 min)

- A7** (a) A J-K master-slave bistable circuit.
(b) A D-type bistable circuit.
(c) An S-R bistable circuit.

Q8 It is required to generate a 4 kHz square-wave signal from a 16 kHz square-wave by using D-type bistables. Sketch a suitable circuit. (4 min)

A8 By connecting the Q output of a D-type bistable circuit to the D input, a simple divide-by-2 circuit is produced. Therefore, the required signal can be obtained by using two D-type bistable circuits connected in series, as shown in the sketch.



Q9 In a table compare synchronous and asynchronous counters for the following criteria:

- maximum speed of operation,
- circuit complexity, and
- ripple-through delay.

(5 min)

A9

	Synchronous	Asynchronous
(a) Maximum speed of operation.	High-speed limited by the propagation delays of the individual bistables. The maximum speed is typically 20 MHz.	Depends on the number of stages in the counter, and is limited by their propagation delay. Maximum speed typically between 50 kHz and 500 kHz.
(b) Circuit complexity.	Contains many gates in addition to the bistable elements.	Simple circuits; few extra gates are required.
(c) Ripple-through delay.	All outputs change simultaneously. There is no ripple-through delay.	Outputs change in turn throughout the counter and this gives rise to considerable delay between the first and last stages.

Q10 Identify the synchronous and asynchronous binary counters from the circuits shown in Figs. 3 and 4. Give your reasons. (2 min)

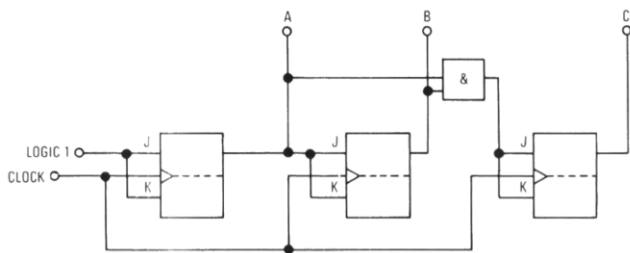


Fig. 3

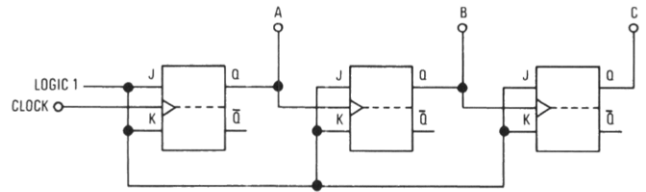


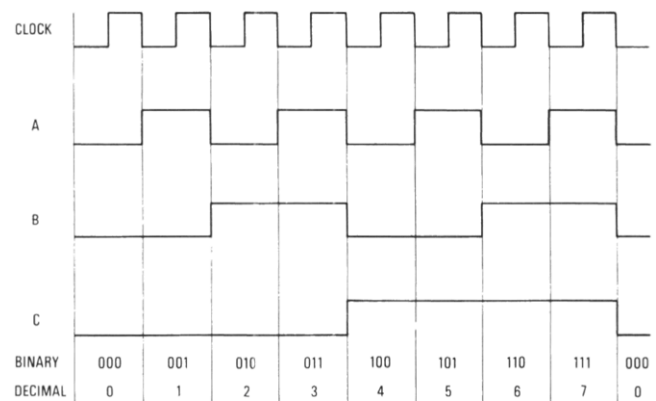
Fig. 4

A10 The circuit shown in Fig. 3 is a synchronous binary counter, and that shown in Fig. 4 is an asynchronous counter.

The synchronous counter can be identified by the connection of the CLOCK which is connected in parallel to each bistable circuit. The clock for each stage of the asynchronous counter is derived from the previous stage.

Q11 Draw the output waveforms for each stage of a 3 bit asynchronous binary counter; show the equivalent binary and decimal count number at each stage. (4 min)

A11



Q12 Explain briefly how an asynchronous binary counter can be made to generate a reverse binary count; that is, the binary equivalent of 7, 6, 5, 4, 3, 2, 1, 0, 7, etc. (1 min)

A12 The simplest way of obtaining a reverse binary count from a binary up-counter is to take the outputs from the Q output of each stage instead of the Q output.

Q13 Fig. 5 shows the pin connections and internal circuit of a 7490 decade counter. Draw a connection diagram showing how it can be used to generate a square wave at one tenth of the frequency of the input clock. Connect pins 3 and 6 to logic 0. (7 min)

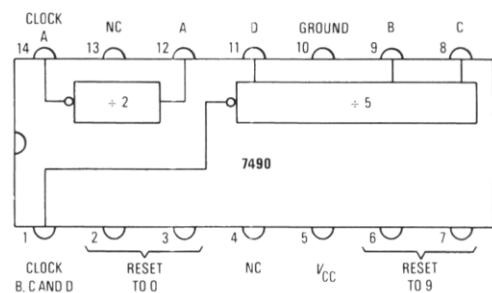
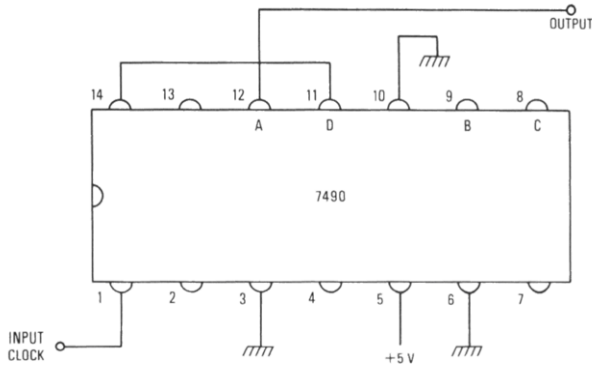


Fig. 5

A13 A circuit which generates a square wave of one-tenth the frequency consists of a divide-by-5 counter followed by a divide-by-2 counter, as shown in the sketch.



Q14 Counters with a large number of stages are readily available in complementary metal-oxide-semiconductor (CMOS) logic. Describe a typical application of such a device. (2 min)

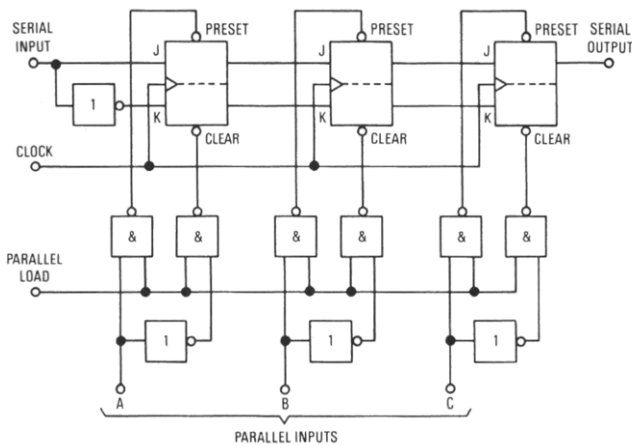
A14 The most common application for a counter with a large number of stages is to divide the high frequency from a crystal oscillator and produce a stable low-frequency waveform. For example, a 21-stage counter could divide a crystal frequency by 2^{21} (2 097 152). Thus a 2.097 152 MHz crystal could be used to generate a stable 1 Hz waveform by using a 21-stage counter to divide its signal.

Q15 Sketch a diagram showing a 3 bit shift register, and indicate clearly

- (a) the serial output,
- (b) the parallel inputs,
- (c) the clock input, and
- (d) the parallel load input.

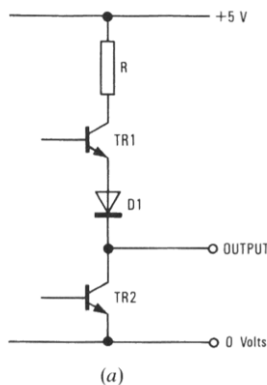
(5 min)

A15



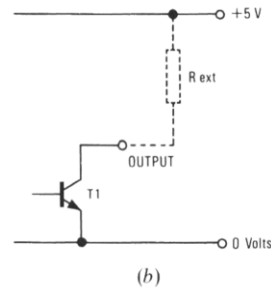
Q16 What is the difference between a 'totem-pole' output and an 'open-collector' output with reference to a logic gate. Illustrate your answer with the circuit diagram of each one. (3 min)

A16 A totem-pole output is the normal output stage of a transistor-transistor logic (TTL) gate. It consists of two transistors, a diode and a resistor as shown in sketch (a).



(a)

The transistors are controlled by the gate circuit and an output driver stage so that under normal circumstances they cannot be ON simultaneously. When transistor TR1 is ON, transistor TR2 is OFF and the output of the gate is taken to logic 1 state. If the base of transistor TR1 is at almost +5 V, then the maximum output is about 3.6 V. When transistor TR2 is ON, transistor TR1 is OFF and the output voltage falls to about 0.2 V. The open-collector output stage is shown in sketch (b).



(b)

Before the open-collector output stage can operate, an external load resistor R_{ext} must be connected to the output terminal. When transistor TR1 is OFF, the voltage rises to about +5 V and, when transistor T1 is ON, the output voltage falls to about 0.2 V.

The advantage of an open-collector output is that a number of gate outputs can be connected to the same load to give a 'wired-OR' connection. However, the totem-pole output has a faster rise-time than the open-collector type.

Q17 Name the logic circuit which could be used as a store for binary numbers in a parallel arithmetic unit, and briefly describe its operation. (4 min)

A17 A suitable circuit is known as a register. It has one D-type bistable circuit for each bit of the number which has to be stored, and a 'load' input which latches the data into the bistables.

Many registers have a control input to enable/disable the outputs from the register. This allows the system of which the register is a part to control the moment at which the data appears on the outputs of the register.

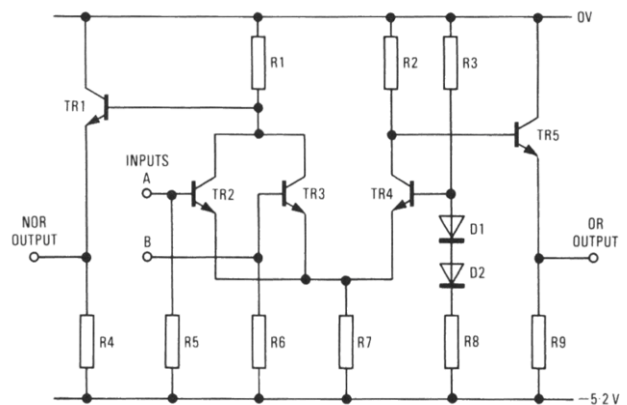
Q18 Briefly explain why emitter-coupled logic (ECL) gates are preferred to complementary metal-oxide-semiconductor (CMOS) or transistor-transistor logic (TTL) gates for certain applications. (2 min)

A18 ECL gates are preferred to both CMOS and TTL gates where very-high-speeds of operation are required.

Typically, an ECL gate has a propagation delay of about 3 ns, compared with 20 ns for TTL and 50 ns for CMOS.

Q19 Many emitter-coupled logic (ECL) functions are based on NOR gates. Draw the circuit of a typical ECL NOR gate. (4 min)

A19



Questions and answers contributed by D. Turner

The following questions are based on the BTEC's standard unit U81/749. Students are advised to read the notes on p. 56

Q1 Label all the parts indicated in Fig. 1, which shows the distribution network between customers and a telephone exchange. (3 min)

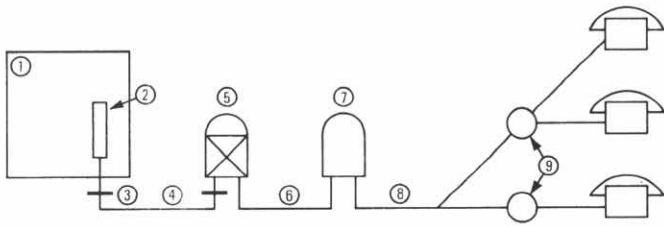


Fig. 1

A1

- 1 Exchange
- 2 Main distribution frame
- 3 Gas seal
- 4 Main cable
- 5 Primary cross-connection point
- 6 Branch cable
- 7 Secondary cross-connection point
- 8 Distribution cable
- 9 Distribution point

Q2 Describe briefly the basic action of a telephone transmitter and receiver. (5 min)

A2 Transmitter

Speech sets up sound waves of alternate compressions and rarefactions in the air. These sound waves impinge upon the diaphragm of the transmitter, which then moves in sympathy with the air pressure. The motion of the diaphragm causes changes in the condition of an electrical circuit, which in turn varies the current flowing in the telephone line. Thus, the energy in the sound waves is converted to electrical energy by the transmitter; the current in the line is an electrical representation of the pressure changes in the air.

Receiver

At the other end of the telephone connection, a varying current flow causes the receiver diaphragm to move and this in turn causes varying pressures on the surrounding air. These variations correspond, for all practical purposes, to those that impinge upon the diaphragm at the transmitter end of the circuit. An approximately similar sound as that spoken is therefore heard by the listener. The receiver thus converts electrical energy into sound energy.

Q3 Name the numbered parts given in Fig. 2. (3 min)

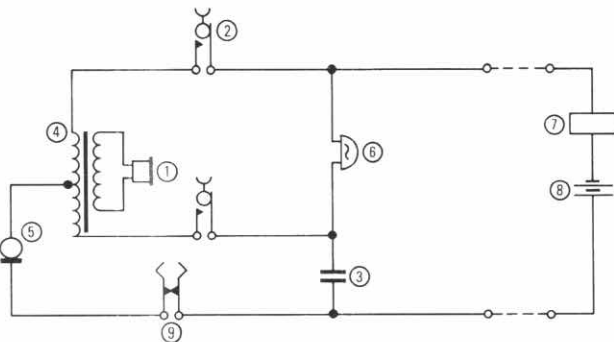


Fig. 2

A3

- 1 Receiver
- 2 Telephone switch-hook springs
- 3 Capacitor
- 4 Induction coil
- 5 Transmitter
- 6 Bell (responds to alternating ringing current)
- 7 Relay
- 8 Battery
- 9 Dial pulsing springs

Q4 What is the primary objective of the local network? Why is the layout complex? (3 min)

A4 The main objective of the local network is to provide a 2-wire metallic or physical connection between two customers. These stations can be situated anywhere within an area served by a local exchange. The local network is complex because it is essential to build in flexibility and economy in the provision of line plant. In this way, demand for connection to the network can be met quickly with a minimum of spare plant lying idle. Flexibility and economy are achieved by dividing the network into two parts, the main and distribution networks, interconnected by cross-connection points.

Q5 (a) State four sources of damage that can occur to cast iron and steel that can impair safety.

(b) Discuss briefly safety aspects of using iron and steel for electrical purposes. (5 min)

- A5** (a) (i) Shocks and blows,
(ii) corrosion,
(iii) overloading, and
(iv) erosion.

(b) Iron and steel are not normally used for the conduction of electricity; other metals, for example, copper and aluminium, give a better performance. However, they are used in the production of high-voltage switchgear and underground electrical plant. Any metals in close proximity to electricity should be bonded together and led to earth. Thus, in the event of a fault or accident, the risk of electrical shocks to people is much reduced.

Q6 What factors are taken into account when a manhole is sited on a trunk route? (3 min)

- A6** (a) Loading within ± 20 m.
(b) Safety measures in relation to the road use.
(c) Visibility.
(d) Danger from flooding.
(e) Proposed road works or improvements which would affect the cable route.
(f) Proximity of other plant.
(g) Effects of creepage.

Q7 State three materials that are used for

- (a) conductors, and
(b) insulators. (2 min)

A7 (a) Any three from copper, aluminium, platinum or silver.
(b) Any three from dry paper, rubber, polyvinyl chloride (PVC) or polyethylene.

Q8 (a) Define resistivity (specific resistance). What formula relates the resistance of a conductor to its physical properties?

(b) A copper wire is 100 m long and has a diameter of 1.0 mm. If the resistivity of copper is $0.0159 \mu\Omega \text{ m}$, calculate the resistance of the wire.

A8 (a) Resistivity can be defined as the resistance between opposite faces of a unit cube of material. The resistance, R , of a conductor is given by:

$$R = \frac{\rho l}{a}$$

where, ρ = resistivity,
 l = length of the conductor, and
 a = cross-sectional area.

(b) The area of the wire = $\pi r^2 = \pi \times 0.5^2 \times 10^{-6} \text{ m}^2$.

$$R = \frac{\rho l}{a} = \frac{1.59 \times 10^{-8} \times 10^2}{\pi \times 0.5^2 \times 10^{-6}} = 2.02 \Omega.$$

Q9 State the properties that solder should possess when it is used for telecommunications work, and the factors to be considered when soldering to make a good connection. What are the main faults that can occur in soldering? (10 min)

A9 Soft solders are of the tin-lead variety; sometimes, they have added properties. Solder for telecommunications work should possess the following properties:

- (a) It should have a lower melting point than the metals to be joined.
(b) It should 'wet' the surfaces to be joined. Insufficient wetting of the surfaces gives rise to poor alloying of the solder with the basic metal and causes high-resistance joints.

(c) It must be free from brittleness and have reasonable mechanical strength.

(d) It must have good electrical conductivity.

(e) For plumbing solder, the plastic range of temperature should allow sufficient time to make a wiped joint. For the soldering of electrical joints, the plastic range should be small to allow quick soldering.

The adhesive strength of a joint depends upon intimate molecular contact between the solder and the metal. This is not possible unless the solder wets the surface of the joint and this cannot occur unless both surfaces are thoroughly cleaned, either mechanically or chemically. A flux must be applied to maintain cleanliness and prevent atmospheric attack.

Factors that ensure a good soldered connection are thus

(a) cleanliness,

(b) correct heating (the temperature of the soldering iron should be approximately 40% above the melting point of the solder), and

(c) the use of the correct flux.

The main faults that can occur in soldering are

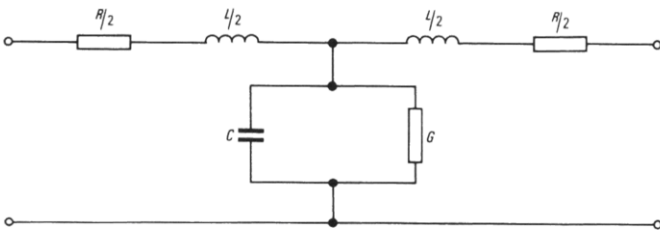
(a) dry joint caused by insufficient heat to make the wire adhere to the tag,

(b) high-resistance joint caused by a crystalline layer between the tag and the wire, and

(c) excess solder, causing a short circuit between tags.

Q10 Draw a simple equivalent circuit diagram of a transmission line; and label and give the units for the primary coefficients.

A10



R = resistance in ohms (Ω).
 L = inductance in henrys (H).
 G = conductance in siemens (S).
 C = capacitance in farads (F).

Q11 What does 'traffic' mean when used in connection with telecommunications? Explain briefly why knowledge of traffic is important in equipment planning. (3 min)

A11 The term is used to describe the amount of telephone or telegraph calls passing through the system. Traffic is the aggregate of calls passing over a group of circuits. Requirements for the provision of exchanges and the trunk cable network can be assessed from the knowledge of the traffic to be carried in the busiest period.

Q12 (a) For many years, lead was the most commonly used material for cable sheaths. What developments led to new types of cable cover?

(b) Explain what is meant by the 'core' of a cable.

(c) List five advantages of polyethylene-sheathed cables over their lead counterparts.

A12 (a) The production of thermoplastic materials with good insulating, dielectric and moisture-proofing properties, and the development of techniques that enabled these materials to be used in the manufacture of cables.

(b) The core of a cable generally refers to everything inside the cable sheath.

(c) (i) Easier to handle,

(ii) cheaper,

(iii) cleaner,

(iv) lighter, and

(v) more flexible.

Q13 (a) Define the term 'telecommunication'.

(b) Give five examples of telecommunication systems.

A13 (a) Telecommunication is the transfer of communication by any electromagnetic means.

(b) (i) Telegraph or Telex.

(ii) Telephony.

(iii) Radio.

(iv) Television.

(v) Facsimile.

Q14 State one advantage of telephony over telegraphy, and one advantage of telegraphy over telephony. (2 min)

A14 Telephony is easy to use and enables users to converse directly together.

With telegraphy, a written record is produced, reception is automatic, no attendance is required at the receiver and only a narrow bandwidth is required.

Q15 (a) How is the speed of a dial controlled?

(b) How are the pulses generated? (5 min)

A14 (a) The speed is controlled by the use of a governor. The governor consists of two wings carrying weights which are forced outwards by centrifugal force. When the governor rotates at correct speed, these weights rub on the walls of a brass cup and the friction prevents any speeding up. The governor is set to allow a speed of 9–11 pulses per second.

(b) As the pulse wheel is rotated, the trigger is moved away from the pulsing springs. When released, they are in contact via an insulated bush and the springs are broken a number of times corresponding to the number dialled. Thus electrical pulses are sent to line.

Q16 What are

(a) bar charts, and

(b) specifications? (3 min)

A16 (a) A bar chart is a form of graphical representation used for indicating the various operations of a project, their duration and their sequence in the overall programme. It provides an immediate visual appreciation of commitment and therefore should be simple, clear, direct and accurate.

(b) Specifications define the requirements of workmanship for the particular installation and the specific requirements for the job.

Q17 Explain briefly the importance of a company having

(a) good industrial relations, and

(b) good customer relations. (3 min)

A17 (a) Good industrial relations are of prime importance: an unhappy labour force is inefficient, unmotivated and poorly productive. Bad relationships lead to loss of earnings for employees and loss of contracts for employers; this can lead to disaster.

(b) Companies should impart a good image to customers; for example, the workforce should be suitably attired, conscientious and polite. A satisfied customer will probably re-engage the company at a later date.

Q18 For a typical national telephone company,

(a) list some of the objectives that it should have,

(b) list activities in a typical cycle of business. (5 min)

A18 (a)

(i) Provision of a sound engineering job.

(ii) Provision of an efficient engineering job.

(iii) Customer satisfaction.

(iv) Attainment of maximum profit.

(v) Attainment of business prestige.

(vi) Provision of good staff relations.

(vii) To keep abreast of new developments.

(viii) To provide maximum return on invested money to shareholders.

(b)

(i) Forecasting future demand.

(ii) Planning and estimating stores, labour and completion time.

(iii) Selling the services to the customer.

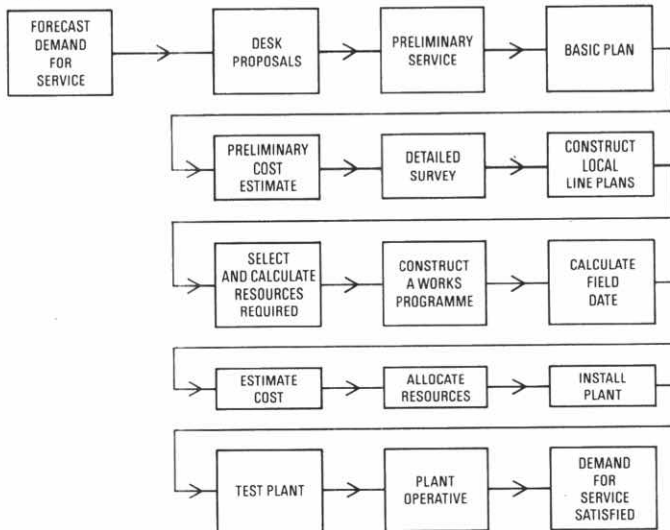
(iv) Executing planned work efficiently and economically.

(v) Collecting accounts.

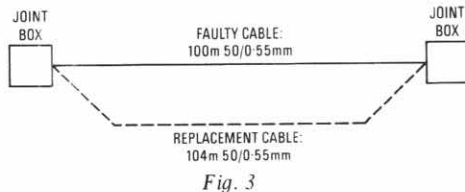
(vi) Reviewing progress and forecasting future demand.

Q19 Draw a block diagram illustrating the sequence of events, from the initial forecast, that takes place to provide service. (3 min)

A19



Q20 Fig. 3 shows the position of a cable fault where it is necessary to renew a length of cable. List the sequence of events for the whole operation. (5 min)



A20 (a) The fault is located; it is established that the length of cable must be renewed.
(b) A suitable length of cable is located coiled on a drum at a cable storage depot.

- (c) The replacement length is tested to prove that it is electrically satisfactory.
(d) The drum is loaded onto a cable carrier vehicle and transported to site.
(e) Both joint boxes are tested for gas and cleaned out. All guards and safety measures are activated.
(f) The existing joints are broken down; a draw rope is attached to the faulty cable and the faulty cable is drawn out.
(g) The faulty cable sheath is examined to discover the reason for the fault.
(h) The new cable is drawn in by using a draw rope, and the cable ends are prepared for jointing.
(i) Replacement cable is jointed to existing cables, and an overall test carried out from the exchange.
(j) Records are updated.
(k) Site is cleared and cleaned.

Q21 Explain what is meant by

- (a) direct labour, and
(b) contract labour.

Under what conditions would each be used? (5 min)

A21 (a) Direct labour refers to where the workforce is totally enlisted from the company. Usage:

- (i) Direct labour can be programmed and controlled.
(ii) In the main, direct labour is more familiar with the plant and work procedures.
(iii) Direct labour may be cheaper for carrying out works of a regular nature.
(iv) Direct labour is employed to do a variety of jobs, whereas contract labour is employed to carry out specific tasks.

(b) Contract labour refers to manpower hired from an outside firm to carry out a specific task at an estimated cost. Usage:

- (i) A company may not have the expertise, equipment, etc. to carry out certain types of specialist work.
(ii) A company may have too much work of its own to do without taking on extra burdens.
(iii) It may be more convenient to use contract labour; for example, on a housing site, where a contractor could install duct and cable together with laying other plant.

Questions and answers contributed by G. Warwick

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